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Design of high frequency circuits for a gigabit per second data transmission system with isolation transformers and improved electrostatic protection

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Design of high frequency circuits for a gigabit per second data transmission system with isolation transformers and improved electrostatic protection

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For the Major Program

To My Father, Mother, and Razan

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

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ABSTRACT

The focus of this dissertation is the design of a 10 Gbit/s wireline data communication system. The data is sent from the driver chip to the receiver chip on a printed circuit board (PCB). In the GHz frequency range, the parasitic effect of various circuits along the signal path affect the quality of the signal sent. Electrostatic Discharge (ESD) protection, PCB traces and packaging increase the signal loss and distortion.

The parasitic effect of ESD protection circuits limits the maximum bandwidth for data transmission. The current high speed driver architectures have the driver circuit directly connected to the chip pads and PCB traces. This causes the chip to be prone to ESD discharge effects. Placing large ESD devices that shunt the output driver to ground, results in their parasitic capacitances acting as low pass filters that severely limit the data transmission rate. The packaging and PCB material are investigated in this project too. An electrical model of the bonding wire is developed through $MATLAB^{®}$ and $HSPICE^{®}$.

In order to increase the data rate, changes in the architecture are performed. The contribution of this project is the introduction of on chip monolithic 4 port RF transformers at the driver and receiver front-end circuits. The transformers act as ESD isolation devices because they filter the low frequency components of the ESD signals before they damage the driver. The driver is physically isolated from the chip exterior. The signal in the driver is conveyed to the traces outside the chip by transformer induction behavior. Spark gap devices are added as ESD discharge paths too. Through investigating several transformer architectures, planar interleaved transformers are fabricated and characterized to have a bandwidth beyond 5GHz needed for suitable data transmission. A design and characterization method of RF transformers by geometric scaling is presented.

The transformers are used in the driver and receiver circuit. Through simulation, the improved design proves to increase the bandwidth of the data link significantly.

CHAPTER 1. High Speed Data Communication

1.1 Introduction

In recent years, a lot of research is focused on improving high speed data communication systems especially in wireline data communication systems. The data rate can reach several Gbit/s. Several products offer around 3 Gbit/s data rate. There are several challenges that have to be met in order to increase the data rate to 10 Gbit/s or more. One of the challenges is the Electrostatic Discharge (ESD) protection devices that are placed at the driver and receiver to protect the chip from ESD events that can be devastating to the chip interior circuitry. The ESD devices, on the other hand, act as low pass filters that filter out the driver transmitted signal above a few GHz. It is very hard to design a chip with no ESD protection because it becomes very vulnerable to ESD events and the yield drops.

Another problem that faces the design of high speed serial link is the signal loss of the path. The path medium in this project is printed circuit board (PCB). The loss of the PCB substrate attenuates the signal after few GHz. If the PCB material is FR4, the signal is attenuated largely in the GHz range.

One of the contributions of this research is to design a high speed serial link with improved ESD protection. The architecture of the driver is to include on chip RF transformers at the driver. The transformers isolate the inner circuitry from outside the chip. The transformers can be designed to have a lower cutoff frequency that is higher that the bandwidth of the ESD signal.

In addition to the transformer, spark gaps are employed at close to the bonding pads where can turn on, the case of ESD event, and constitute an alternate path for the ESD current to pass through them to ground. The design of a serial link with on-chip RF transformers requires

encoding and decoding schemes that incorporate the special characteristics of the transformers.

1.2 Background

The speed of light is around 3×10^8 m/s. If data is to be transmitted between two chips on a printed circuit board (PCB) at a high rate, then the speed of light should be taken into consideration. In [54], an NRZ (Non-return to Zero) data rate of 10 Gbit/s/pin was achieved in CMOS 0.18u technology. This NRZ data rate needs a clock of 5 GHz, and a total bit rise time, and flat time of around 100ps . The bit rise time is about 50ps. To transmit this signal on a PCB, the speed of a signal in the interconnect needs to be determined. It depends on the shape of the interconnection if it's a microstrip line (MSL) or a strip line (SL) and is inversely proportional to the square root dielectric constant of the laminate material of the PCB. This speed is typically around 1/4 to 1/3 of the speed of light. If a signal is to travel around 10 inches then it needs around 1.7ns, which is much longer than the bit time (100ps). This leads to having more than one bit in flight between the transmitter and the receiver.

It can be deduced that high frequency and microwave design techniques must be used in the design phase. This includes broadband matching, broadband RF transformer design, interconnect design, device parasitic effects. Many design issues that were not taken into consideration at low frequencies are important now. The problem of high-speed digital data transmission design becomes both an analog and mixed design issue in addition to a microwave design issue.

1.3 Prior art

There are several approaches to achieve wired point-to-point high-speed data communication systems. The approach depends also on the type of interconnection between the chips. The link might be fiber optical, microstrip line, or strip line. It also depends on the driver and receiver design. In [16], two different approaches are described. The first is the voltage mode , while the second is current mode [58]. The current mode (CM) approach is chosen over the voltage mode (VM) approach [6], [31]. This is due to the fact that CM provides bet-

ter noise immunity, less power consumption, less chip area, less delay, and other advantages. A 700Mbps/pin was achieved using current mode logic [57], while 10Gbit/s/pin on a 0.4um CMOS technology was reached in [23].

In this project, a high-speed data transmission system is being developed such that it achieves high speeds, around 10-15 Gbit/s/pin at the same time it takes into consideration the circuit protection needs.

1.4 This project

This project is about designing a high-speed data transmission scheme between two chips on a printed circuit board. This includes several design blocks in the driver and the receiver. A schematic is shown in Figure 1.1.

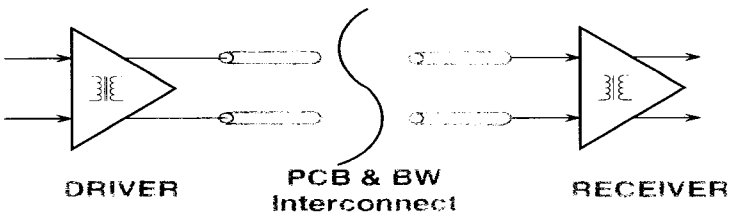

Figure 1.1 Data transmission scheme with transformers

In the driver chip, there are two encoders for the data before being sent. One encoder is for the DC balancing of the data on the interconnection to prevent DC line wandering problem. The other encoder is designed and integrated into the multiplexer in order to focus the energy content of the signal transmitted around certain frequency. In this way, a termination scheme using mere resistors would be easier to implement at the transmitter and the receiver.

The ESD problem is addressed in the transmitter and the receiver. The mechanism of ESD protection is to provide an alternate path for the current spark to be discharged to the substrate of the chip instead of getting to the internal circuitry and damaging active devices and passive devices. The classical ESD protection scheme is to place two diodes operating in reverse mode in the normal operating condition. When a high voltage spark is affecting the circuit through the pads, then large diodes would become conductive and constitute an

alternative current path for the charge. It should be noticed here that the gate or drain of a transistor is only insulated from the interconnection metal by a very thin layer of Silicon dioxide layer, (less than 80 Angstroms).

In the proposed scheme, a transformer is placed at the transmitter and receiver as an interface and as an insulator between the chip internal circuitry and the PCB interconnect as in Figure 1.2. The transformer differentiates the current signal that enters its primary and then generates an induced voltage at the secondary ports of the transformer. To divert the spark from affecting the internal circuitry, spark gap structures are placed close to the chip pads and have a pointing shape that are close to the interconnection so that a spark can be formed between the interconnect and the spark gap. In this way, a conductive path is generated when a huge voltage affects the chip. This path consists of the interconnection that reaches the chip pads from outside, the chip pads, the spark that is formed by ionizing the air or the insulation between the interconnection and the spark teeth, a connection between the spark gaps and the substrate.

In addition to spark gaps, special care was taken into designing broadband transformers. The transformers need not have high selectivity factor. This is because the energy content of the data can have a spectrum of frequencies instead of one frequency. In this way, the task of designing monolithic transformers becomes less challenging because of the lower selectivity factor. Nevertheless, the transformer needs to have a high resonant frequency to behave in an inductive way in the frequency range of interest. In this project, a broadband frequency model of the transformer is being developed.

The chip is attached on the PCB using Chip on Board (COB) attachment method. With COB, the bare chip is attached directly on the PCB using a layer of glue. The chip is not packaged because package leads need to be avoided in this design due to the filtering effect they have on high frequency components of signals. Therefore less parasitic capacitance and inductance is introduced into the interconnection. The other advantage is improved ground bounce immunity of the design. In this way, the ground potential won't be subject to changes due to the current that passes through the wires. One more advantage of COB is that less

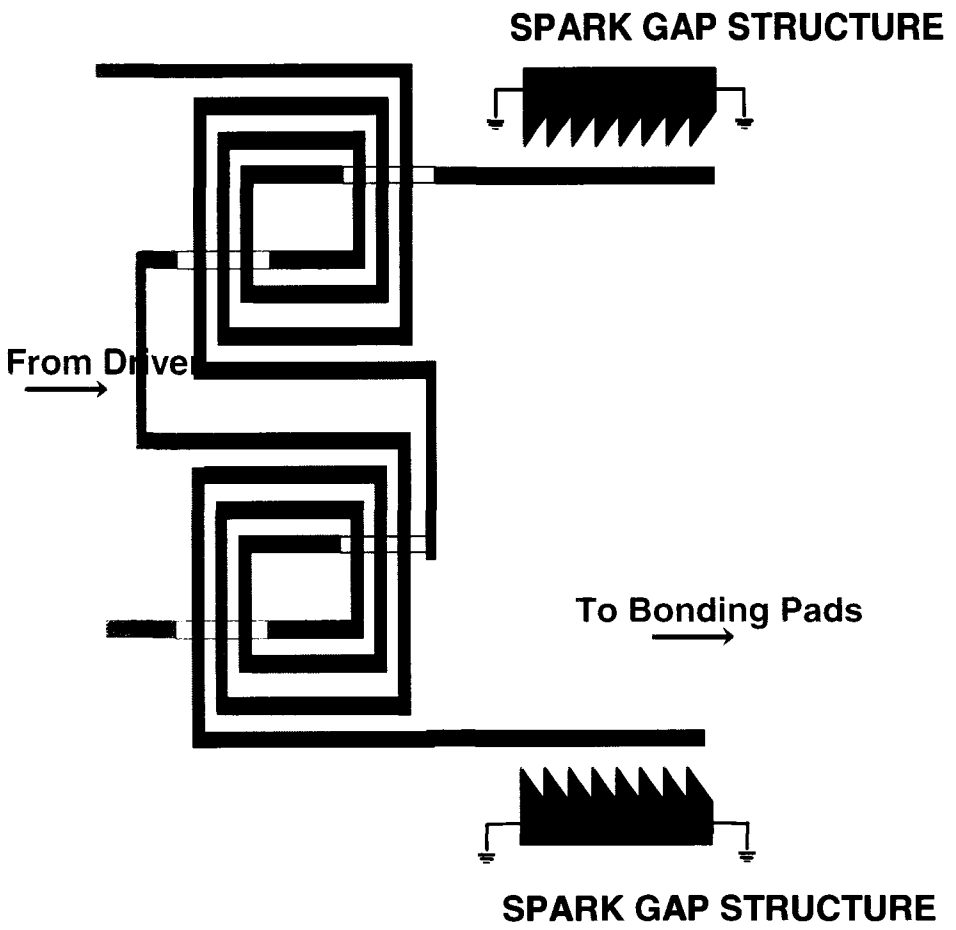

Figure 1.2 Transformer with spark gap structures

discontinuity problems are faced through data transmission. This means a less noisy signal is transmitted.

Bonding wire modelling is part of the high-speed data transmission design. What is needed is a broadband frequency model of the interconnection between the driver and the receiver circuitry. Modelling of the bonding wire between the chip and the printed circuit board was necessary to simulate the link. A model was developed using HSPICE Field Solver simulator.

An improved laminate material used in the fabrication of PCBs was chosen for this project. This material, GML1000, provides a low and stable dielectric constant, and therefore low loss for signals transmitted on the PCB. The low loss of the material would allow to reduce the requirements on pre-emphasis equalizer blocks at the transmitter and receiver, respectively.

1.5 Organization of this dissertation

In the first chapter a method for designing RF inductors and transformers by geometric scaling. This method can be used to design on-chip RF inductors and transformers without the need for expensive high frequency electromagnetic simulators or high frequency characterization equipment.

The second chapter discusses the method for designing several types of high frequency transformers, and ways to improve their bandwidth. Layout techniques, in addition to calibration and decoupling methods, are provided. A software interface between the transformer design software, ASITIC, and MATLAB, is introduced to help is speeding up the design process, and optimizing the electrical parameters of the designed transformer.

A special type of transformers, the toroidal transformer, is explored in the next chapter. Several modifications to the toroidal transformer structures are made so as to increase the transformer bandwidth. The choice of PCB that was used, with a brief comparative study between several PCB types, is presented in Chapter 5.

Chapter 6, discusses Bonding Wires (BW). A BW modelling and design software is introduced. The software provides an electrical model, in HSPICE, for the transformer in the GHz range using the W model. This electrical model can be used in simulating the serial link in HSPICE. In addition, the BW software provides analysis of the characteristic impedance of the BW pair and the total amount of parasitic inductance and capacitance in it.

The next chapter provides the design of high frequency transformers as ESD protection devices. In addition, spark gaps work as ESD protection devices that provide an alternate path for the ESD charge instead of damaging the internal circuitry.

The Driver chapter provides encoding methods for the driver of the serial link. Two encoding schemes are introduced. These include driver encoder and bus encoder. In addition, broadband matching is discussed.

CHAPTER 2. Design of RF inductors in CMOS 0.18μ by geometric scaling

2.1 Abstract

In this chapter, research results about design and characterization of geometrically scaled RF inductors and transformers are presented in comparison to an Electromagnetic (EM) simulation, and to on-chip design and characterization results. The geometries of the on-chip inductor are scaled up by a factor α. The scaled up model is characterized at a scaled frequency range of $1/\alpha$. When the frequency is scaled back to the original range, the scattering parameters extracted from the scaled model reflect the behavior of the original on-chip model. A set of geometrically scaled models are compared to simulations in ASITIC[43]. The characterization results show an agreement in S_{11} within 6.7%, and in f_{res} within 17.4%. On-chip RF inductors were fabricated in a CMOS 0.18μ technology while the scaled models were fabricated on a flexible circuit material with 2oz and 3oz copper. The characterization results show an agreement in S_{11} within 8% and in resonance frequency within 20%.

2.2 Introduction

Nowadays, there is considerable research focusing on design and characterization of on-chip RF inductors fabricated on silicon integrated circuits. The design and characterization of RF inductors can be a considerable task with fabrication time lasting for weeks. The fabrication of the RF inductors can be expensive due to the large chip area occupied by test and calibration structures. Simulation of RF inductors that have non-rectilinear geometries can be computationally intensive for the electromagnetic simulator (EM) simulator especially

if a large number of frequency points are required. In this chapter, a method is presented for predicting the behavior of RF inductors before fabrication by the method of geometric scaling (GS). The GS method can help in achieving a single pass design.

The organization of this chapter is as follows. This section describes the GS method and the effect of geometry and frequency scaling on the electrical parameters of the RF inductor equivalent electrical model. Afterwards, a geometrically scaled RF inductor is characterized and compared to the original model in ASITIC. Then an on-chip characterized inductor is compared to a geometrically scaled RF inductor. Afterwards, sources of error, and approximations are discussed. This chapter is concluded with a summary of the results obtained through this research.

This research uses the concept of dimensional analysis by Buckingham [10], and [11]. The basic idea is to scale the geometries of the on-chip RF inductor by a scaling factor α in the x, y, and z direction. This new dimension should be comparable to traces that can be etched on a copper clad laminate or a rigid printed circuit board. As a result, the frequency range of the new scaled inductor is reduced by the same factor α, and the scattering parameters are extracted for the scaled model. Afterwards, the frequency range of the extracted scattering parameters is scaled up by the factor α to return to the original on-chip frequency range. As for the magnitude and phase of S parameters, they are left unchanged. This new scaled parameter set reflects the behavior of the on-chip RF inductor at the original operating frequency. As a result, expensive test equipment calibrated to several GHz frequency range is not needed for this measurement.

The geometric scaling of the on-chip RF inductors is not completely cancelled out by the frequency inverse scaling [3]. Figure 2.1 presents an electrical model of the on-chip inductor [69], and Table 2.1 lists the model electrical parameters where ρ_m and ρ_{si} are the resistivity of the conductor and substrate respectively, l, w, t and are the length, width, and thickness of the conductor respectively.

Q is the mutual inductance parameter that depends on the geometric mean distance between the conductor segments, ε_{ox}, and ε_{si} are the dielectric material constants for the oxide

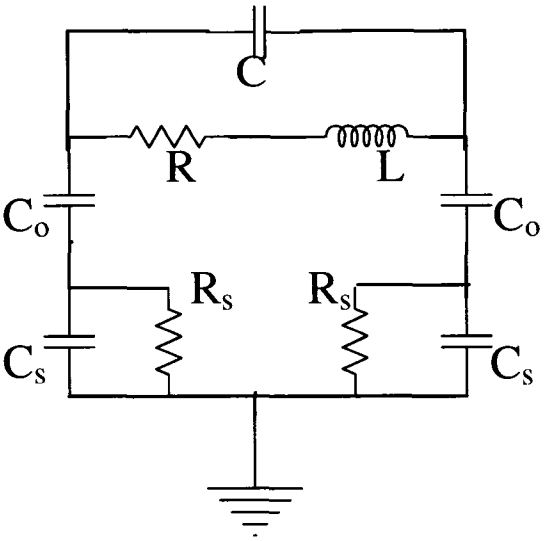

Figure 2.1 Inductor electrical model

layer and the substrate respectively. t_{ox} and h_{si} are the oxide thickness and the substrate thickness respectively. α is the scaling factor defined as the new geometrical dimension over the old geometrical dimension. The effect of scaling on the model electrical parameters is shown in the second column of Table 2.1.

While the capacitances C_{ox} and C_{si} do scale up by a factor α, as in equations D and E, Z_C remains essentially unchanged because the scale of α in C is cancelled by the $1/\alpha$ scale in the frequency. Similarly, as the inductance L scales up by a factor α, as in equation B, Z_L remains unchanged because the scale of α in L is cancelled by the $1/\alpha$ scale in the frequency.

Note that geometric scaling by α affects R_s and R_{si} because there is obviously no frequency component in the ideal resistor model. As a result, additional resistance should be added to the scaled model resistance to reflect the actual resistance of the original model. This resistance is equal to:

$$\begin{aligned} R_{\text{compensation}} &= R_{\text{on chip}} - R_{\text{scaled model}} \\ &\simeq R_{\text{on chip}} \end{aligned} \tag{2.1}$$

since $R_{\text{geom scaled}} \ll R_{\text{on chip}}$. Compensation for the resistance can be done by adding chip resistances (lumped or distributed) to the geometrically scaled model before scattering pa-

rameters are extracted. Another compensation method is to add the compensation resistors mathematically after scattering parameters extraction.

Table 2.1 Inductor electrical parameters

Parameters	Scaled Parameters	Eqn.	Ref.
$R_s \cong \frac{\rho l}{wt}$	$R_s \cong \frac{1}{\alpha} \cdot \frac{\rho l}{wt}$	A	[69]
$L = 2l\left\{ln\left(\frac{2l}{w+t}\right) + 0.5 + \frac{(w+t)}{3l}\right\}$	$L = 2l\left\{ln\left(\frac{2l}{w+t}\right) + 0.5 + \frac{(w+t)}{3l}\right\}$	B	[69]
$M = 2lQ$	$M = \alpha \cdot 2lQ$	C	[69]
$C_{ox} = \frac{1}{2}\frac{\varepsilon_{ox} wl}{t_{ox}}$	$C_{ox} = \alpha \cdot \frac{1}{2}\frac{\varepsilon_{ox} wl}{t_{ox}}$	D	[69]
$C_{si} = \frac{1}{2}\frac{\varepsilon_{si} wl}{h_{si}}$	$C_{si} = \alpha \cdot \frac{1}{2}\frac{\varepsilon_{si} wl}{h_{si}}$	E	[69]
$Z_L = jwL$	$Z_L = j\frac{2\pi}{\alpha} f \cdot \alpha L = jwL$	F	
$Z_C = \frac{1}{jwC}$	$Z_C = \frac{1}{j\frac{2\pi}{\alpha} f \alpha C} = \frac{1}{jwC}$	G	

2.3 Simulations of RF inductors in ASITIC

In this example, an on-chip inductor is geometrically scaled up by a factor α. The scaled up inductor is fabricated on a flexible printed circuit material such as Pyralux® from Dupont®. It is a copper clad laminate. α depends on the thickness of the on-chip inductor metal layer $t_{\text{on-chip}}$, and the metal layer thickness of the scaled up model t_{PCB}. It is calculated as

$$\alpha = \frac{t_{\text{PCB}}}{t_{\text{on-chip}}}. \tag{2.2}$$

The scaled model is built on a thick substrate that presents a scaling of the original on-chip substrate. It has the same dielectric constant of the original substrate. A fabrication step for the scaled model, such as etching of the copper clad laminate, is easily performed. Another method is to use a rigid PCB and mill the traces on it and remove the extra copper. Figure 2.2 presents the scaled up model of the inductor fabricated on flexible printed circuit material for

$\alpha = 204$. Figure 2.3 shows the scaled model for $\alpha = 136$. To simulate the effect of dielectric material between the transformer and the substrate, a Kapton® sheet was placed between the transformer and a wafer on top. The wafer represents the loss that the inductor experiences from the substrate in its original on chip model. The wafer's resistivity is scaled relative to the chip substrate.

The scaled model is then characterized over a frequency range that is the original desired frequency range through two port S parameter measurements [67], as shown in Figure 2.5, and Figure 2.6. Since resistance is not scaled with scaling geometry, compensation resistances are added mathematically to the scaled model after characterization. The inductor was simulated in ASITIC [43] as in Figure 2.4.

For $\alpha = 136$, the scaled model is compared to the original simulated model in Table 2.2 in terms of f_{res}, and $S_{11,res}$. f_{res}, the resonant frequency of the original model, is 14.8 GHz. f_{res}, the resonant frequency of the measured model, is 99.9 MHz. When scaled back, f_{res} is 13.6 GHz. Compared to $f_{res} = 14.8$ GHz, the percentage error in f_{res} is 8.11%. $S_{11,res}$ of the original model is 0.819. $S_{11,res}$ of the measured model is 0.872. Compared to $S_{11,res} = 0.872$, the percentage error in $S_{11,res}$ is 6.47%.

For $\alpha = 204$, the scaled model is compared to the original simulated model in Table 2.3 in terms of f_{res}, and $S_{11,res}$. f_{res}, the resonant frequency of the measured model, is 59.9 MHz. When scaled back, f_{res} is 12.22 GHz. Compared to $f_{res} = 14.8$ GHz, the percentage error in f_{res} is 17.4%. $S_{11,res}$ of the measured model is 0.834. Compared to $S_{11,res} = 0.834$, the percentage error in $S_{11,res}$ is 1.83%.

Table 2.4 presents the inductances for $\alpha = 1$, $\alpha = 136$, and $\alpha = 204$ for the frequency range of $1 - 4$ GHz. The percentage error in L is $< 9.6\%$ for $\alpha = 136$, and is $< 2.25\%$ for $\alpha = 204$. The low error represents the good agreement between the scaled model and the original model.

2.4 Practical design: On-Chip RF inductors

Two RF inductors were fabricated in a CMOS 0.18μ process with non-epi substrate. Inductor A (L_A) is fabricated in a metal layer of nominal thickness of $0.5\mu m$, and occupies an

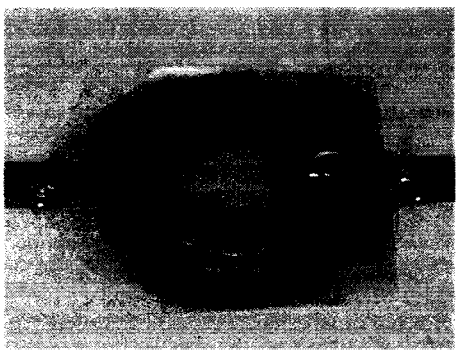

Figure 2.2 Inductor scaled by $\alpha = 204$

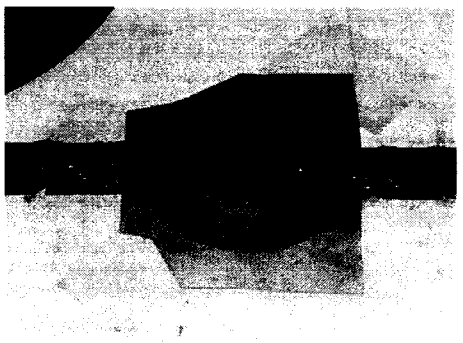

Figure 2.3 Inductor scaled by $\alpha = 136$

area of 220μm$\times 220\mu$m while Inductor B (L_B) is fabricated in a metal layer of $1\mu m$ nominal thickness and occupies a similar area. The inductors are characterized using a Agilent E8364A 50GHz vector network analyzer. The GS method is implemented on (L_A). In the case of (L_A), two scaled models are implemented for 2oz and 3oz copper clad laminates. For $t_{\text{PCB}} = 2$oz and $t_{\text{PCB}} = 3$oz, $\alpha = 140$ (nominal), and $\alpha = 210$ (nominal) respectively. A photo of (L_B) scaled on 3oz is shown in Figure 2.14. A dielectric layer is placed on the scaled inductor to

Table 2.2 Measured results at $\alpha = 136$

Inductor	$\alpha = 1$	$\alpha = 136$		
		Measured model	Scaled back	%err
f_{res} GHz	14.8 GHz	99.9 MHz	13.6 GHz	8.11
$S_{11,res}$	.819	.872	.872	6.47

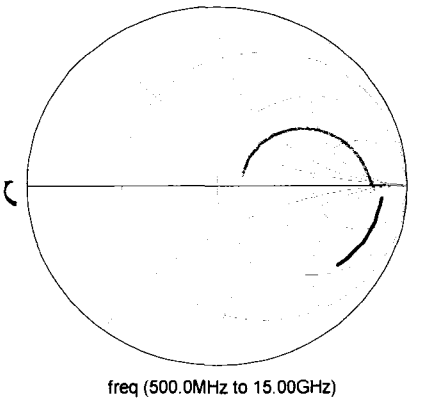

Figure 2.4 Inductor simulation in ASITIC

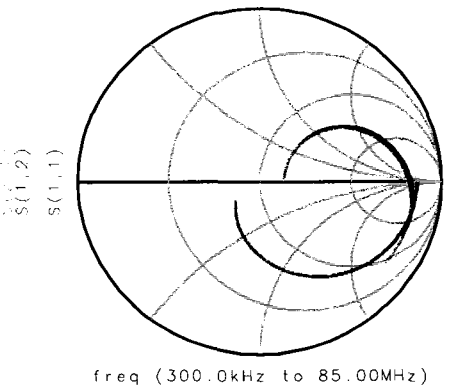

Figure 2.5 Measured S parameters at $\alpha = 204$

simulate the scaled dielectric thickness between the on-chip inductor and substrate. Then, a wafer that had a scaled resistivity of the original substrate was placed on top to simulate the loss due to substrate coupling. The scaled model is then characterized over a frequency range that is $1/\alpha$ the original desired frequency range through two port S parameter measurements [67]. Finally, the frequency range is scaled-up back to the original frequency range.

2.4.1 Inductor in 0.5μ m metal layer

Note that for all the various figures that are presented, X's are for 2oz and O's are for 3oz while solid black line presents on-chip inductor data. For (L_A), Figure 2.8 shows a Smith *Chart*® plot of S_{11}. Figure 2.8 presents the effective quality factor of (L_A) where it is calcu-

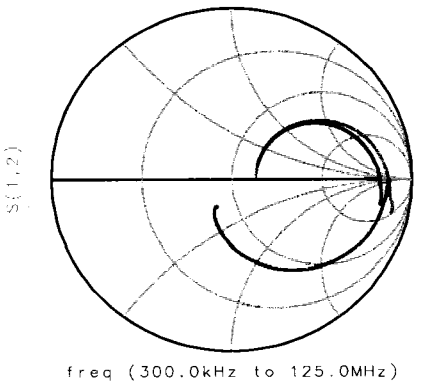

Figure 2.6 Measured S parameters at $\alpha = 136$

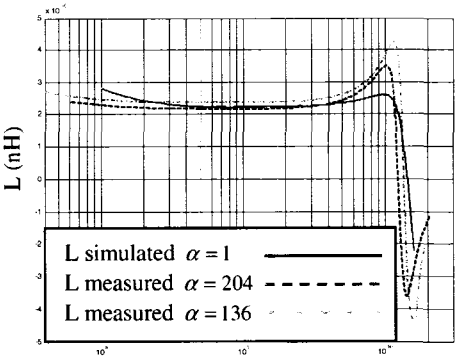

Figure 2.7 Inductance of original and scaled models

lated as

$$Q_{eff} = \frac{Imag\,(Z_{in})}{Real\,(Z_{in})} \tag{2.3}$$

where is the input impedance seen looking into the inductor,. The effective inductance calculated as:

$$L_{eff} = \frac{Imag\,(Z_{in})}{2\pi f} \tag{2.4}$$

is shown in Figure 2.10. It should be noted that L_{eff} includes the effect of parasitic capacitances on the inductor structure.

Table 2.5 lists characterization results of the scaling on Inductor (L_A). As for f_{res}, the percentage error %err was relatively low, $< 5\%$, while %err in $|S_{11,f_{res}}|$ was $< 8\%$. The %err in L was $< 22\%$ for 2 GHz $< f <$ 6 GHz for 2oz model, but for the 3oz model, it was $< 34\%$

Table 2.3 Measured results at $\alpha = 204$

Inductor	$\alpha = 1$	$\alpha = 204$		
		Measured model	Scaled back	%err
f_{res} GHz	14.8 GHz	59.90 MHz	12.22 GHz	17.4
$S_{11,res}$	.819	.834	.834	1.83

Table 2.4 Inductance for $\alpha = 1, 136$, and 204

L (nH)	$\alpha = 1$	$\alpha = 136$	% err	$\alpha = 204$	% err
@1GHz	2.22	2.37	6.76	2.17	2.25
@2GHz	2.23	2.39	7.17	2.18	2.25
@3GHz	2.26	2.44	7.96	2.23	1.33
@4GHz	2.29	2.51	9.6	2.32	1.31

for the same frequency range. As for %err in $f_{Q_{max}}$, and Q_{max} it was $< 5\%$, and $< 18\%$ respectively for the 2oz model. This is a better result than the 3oz model which has 25% and 43.1% for $f_{Q_{max}}$, and Q_{max} respectively.

Note that L, and Q_{max} gave a pessimistic prediction for the on-chip inductor parameters. These scaled model can be considered as a lower bound compared to the original on-chip model.

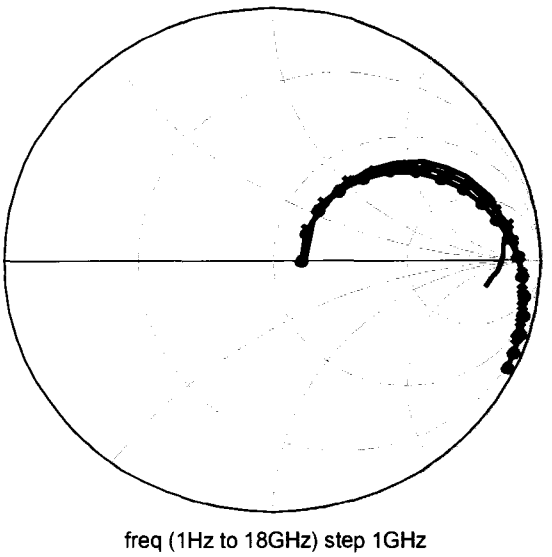

Figure 2.8 S_{11} for inductor (L_A)

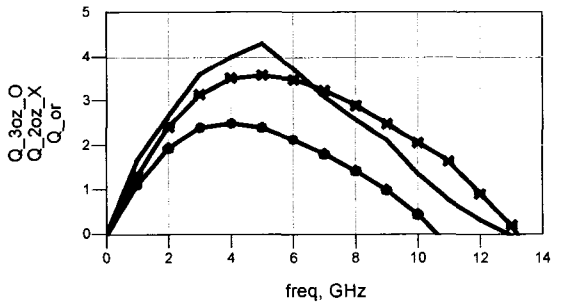

Figure 2.9 Q factor of on-chip and scaled inductor (L_A)

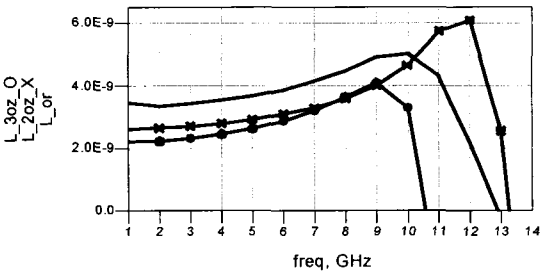

Figure 2.10 L_{eff} of on-chip and scaled inductor (L_A)

2.4.2 Inductor in 1μm metal layer

For (L_B), Figure 2.11 shows a Smith Chart plot of S_{11}. The effective quality factor is presented in Figure 2.12. In addition, Figure 2.13 demonstrates L_{eff}.

Table 2.6 lists characterization results of the scaling on Inductor (L_B). As for f_{res}, the percentage error %err was lower for the 3oz than for 2oz, while %err in $|S_{11,f_{res}}|$ was $< 4.5\%$. The %err in L was lower in the case of 2oz, $< 8\%$, than for 3oz, $< 17.3\%$ for 2GHz$<f<$6 GHz.

Note that $f_{Q_{max}}$, and Q_{max} give a pessimistic prediction for the On-chip inductor parameters. These scaled models can be considered as a lower bound compared to the original on-chip model.

2.5 Sources of error

There are several sources of error that contribute to the deviation of the results from the actual values. The network analyzer was calibrated using low frequency connectors. This

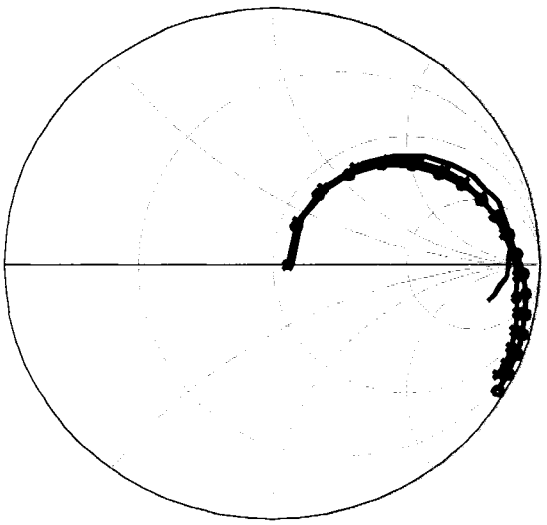

Figure 2.11 S_{11} for inductor (L_B)

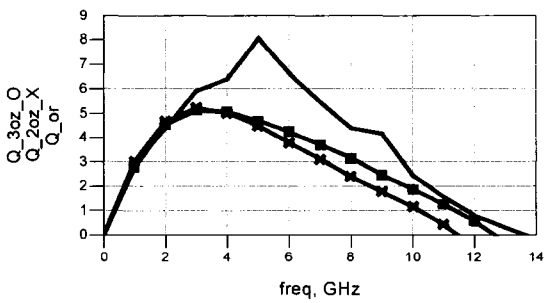

Figure 2.12 Q factor of on-chip and scaled inductor (L_B)

calibration can be improved by using higher frequency connectors. In addition, it is more difficult to find wafers that are thick enough to capture the substrate loss effect. A substrate with the desired scaled resistivity was not available at the time of the experiment. A substrate with a scaled resistivity within a range of the desired resistivity, was used. This resulted in different parasitic capacitances that affected the electrical parameters of the inductor such as $f_{Q_{max}}$, and also generated loss that affected Q_{max} for the scaled models. Also, the equations in Table 2.1 are approximations of the actual behavior of the inductor; the skin effect was not taken into consideration when modelling R_s, and a constant resistance was assumed for the metal winding for the whole frequency range of operation. This in turn affects Q_{max}.

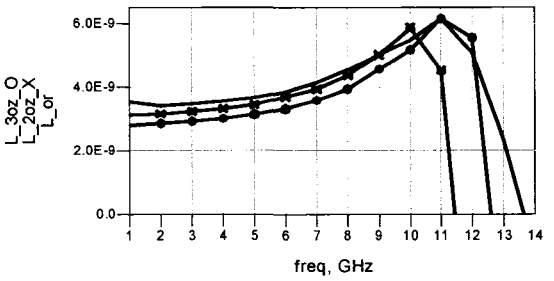

Figure 2.13 L_{eff} of on-chip and scaled inductor (L_B)

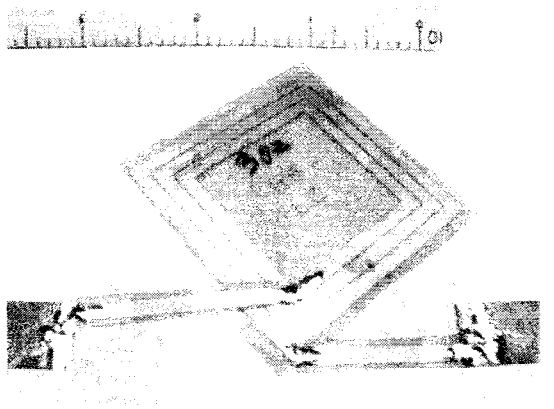

Figure 2.14 Photo of scaled inductor (L_B) on 3oz

In addition, the inductance was calculated as in Equation 2.4. This included the parasitic capacitances of the structure. This means that the choice of the substrate that simulates the loss affects the value of L_{eff}. The method can use offset cancellation techniques to cancel most of the errors in Q_{max} and $f_{Q_{max}}$.

2.6 Contribution summary

In this chapter, a method of characterization of RF inductors by geometric scaling is presented. The geometries of on chip passive RF components are scaled up by a factor α. The scaled model is characterized at a scaled down frequency range by a factor $1/\alpha$. The scattering parameters extracted from two geometrically scaled-up model at the scaled-down frequency range showed good agreement with the original on-chip inductors at the original desired fre-

Table 2.5 Data presenting on-chip and scaled models of inductor (L_A)

Inductor (L_A)	On-chip	2oz	%err	3oz	%err
f_{res}, GHz	12.8	13.2	3.1	12.2	4.69
$\|S_{11,f_{res}}\|$, GHz	0.852	0.918	7.8	0.915	7.39
L,nH @2GHz	3.34	2.65	21.1	2.22	33.5
L,nH @4GHz	3.56	2.79	21.7	2.45	31.2
L,nH @6GHz	3.87	3.09	20	2.87	25.7
$f_{Q_{max}}$, GHz	5.04	4.82	4.37	3.78	25
Q_{max}	4.38	3.61	17.6	2.49	43.1

Table 2.6 Data presenting on-chip and scaled models of inductor (L_B)

Inductor (L_B)	On-chip	2oz	%err	3oz	%err
f_{res}, GHz	13.68	11.49	16	12.7	7.2
$\|S_{11,f_{res}}\|$, GHz	0.877	0.903	2.9	0.916	4.47
L,nH @2GHz	3.4	3.13	8	2.82	17.3
L,nH @4GHz	3.55	3.29	7.48	2.97	16.32
L,nH @6GHz	3.86	3.66	5.0	3.3	14.5
$f_{Q_{max}}$, GHz	5.04	3.29	34.7	3.2	36
Q_{max}	8.07	5.31	34.2	5.19	35.7

quency range. Extra parasitic capacitances that do not have any equivalence on-chip, reduced the effective inductance. The models gave also a lower bound for Q_{max} and $f_{Q_{max}}$. This method can be utilized to give a prediction for RF spiral inductors before fabrication. While the equations given in Table 2.1 are primarily for lumped circuit elements, the same scale factor applies to distributed circuits, and work with distributed circuits will continue.

CHAPTER 3. Design and characterization of RF transformers with improved bandwidth

3.1 Introduction

Transformers (TR) are vital elements in this project. They have several responsibilities. They act as an interface between the transmitter chip and the PCB interconnections. In addition, they act as a protection device for the chip. Since digital data is transmitted through the TR to the PCB microstrip line (MSL), the transformer needs to be capable of passing a wider range of frequency contents of the signal compared to typical RF TR's which pass a narrow band of frequencies and need to have a high selectivity factor. There are several monolithic planar transformer structures such as planar interleaved 4 port transformers, bandwidth improved RF transformers, and other structures that are discussed in this chapter.

3.1.1 Organization of this chapter

Analysis of ideal 2 port and 4 port transformers is presented in the next section. Then a description of the resonance frequencies of the transformer follows. Afterwards, an analysis of changing the metal layer for the transformer and its effect on the transformer electrical parameters, is given. Next, the objective of research is presented. Several transformer structures are discussed such as planar interleaved, concentric, and ring transformers. Analysis of bandwidth improved transformers is presented too. An interface that helps in the design of RF transformers between MATLAB and ASITIC, is introduced. Methods for probe recalibration and pad parasitic decoupling capacitances extraction, are explained afterwards. Then characterization results are given for planar transformers characterized in a 0.18μ CMOS process.

3.2 Scattering parameter analysis of ideal RF transformers

In this section, a brief analysis is presented about the behavior of the ideal RF transformer in the form of S parameters. Analytical expressions for 2 port and 4 port ideal RF transformers are developed with supporting figures.

3.2.1 Analysis for ideal two port transformers

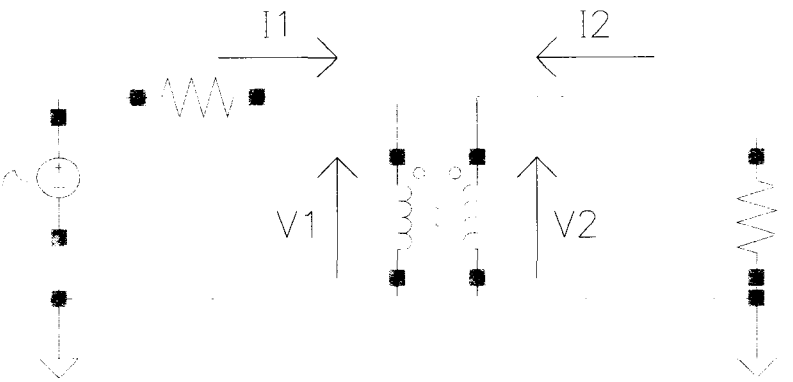

Figure 3.1 Schematic for 2 port ideal transformer

Table 3.1 Two port ideal transformer parameters

Parameter	Definition
I_1	Current entering the transformer primary
I_2	Current entering the transformer secondary
V_1	Voltage across the transformer primary
V_2	Voltage across the transformer secondary
L	Self inductance of the primary or secondary
M	$=k\sqrt{L^2}$
ω	$=2\pi f$, f is the frequency

Figure 3.1 presents a schematic for an ideal transformer where the S parameters are to be calculated. The parameters needed for S parameters calculations are listed in Table 3.1. Table 3.2 lists the electrical parameters for the ideal two port transformers. S_{11} can be calculated as:

$$S_{11}|_{V_2=-I_2Z_2} = \frac{V_1 - I_1 Z_1^*}{V_1 + I_1 Z_1} \tag{3.1}$$

$$= \frac{\omega^2 M^2 - \omega^2 L^2 - 2500}{\omega^2 M^2 - \omega^2 L^2 + 2500 + j100\omega L} \tag{3.2}$$

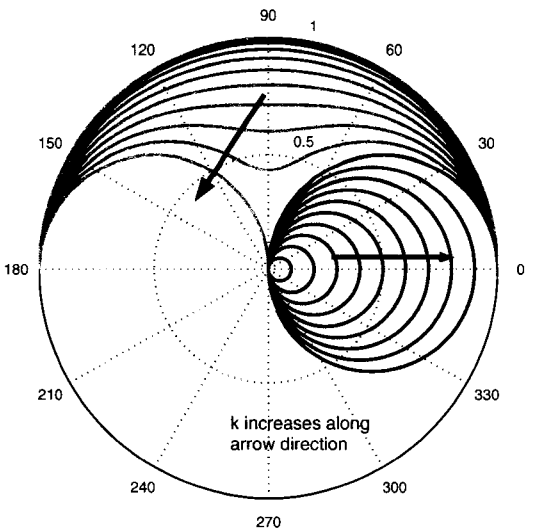

Figure 3.2 S parameters of ideal 2 port transformer on a polar scale, S_{11} in red, and S_{21} in blue

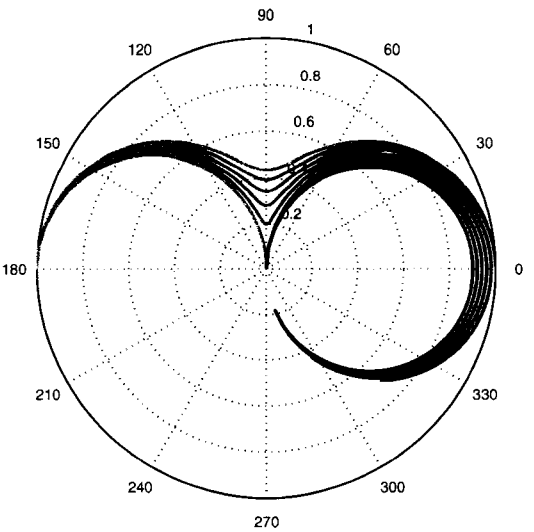

Figure 3.3 S parameters of ideal 2 port transformer on a polar scale, S_{11} in red, and S_{21} in blue, $k = 0.8$ to 1

For $\omega \to 0$,

$$S_{11}(\omega \to 0) = 1\angle 180 \tag{3.3}$$

which represents a short circuit; total reflection at the primary. While for $\omega \to \infty$,

$$S_{11}(\omega \to \infty) = \lim_{\omega \to \infty} \frac{\omega^2 M^2 - \omega^2 L^2}{\omega^2 M^2 - \omega^2 L^2 + j100\omega L} \tag{3.4}$$

$$= 1\angle 0 \tag{3.5}$$

which represents an open circuit. As for S_{21}, it can be calculated as:

$$S_{21}|_{V_2=-I_2Z_2} = \frac{V_2 - I_2 Z_2^*}{V_1 + I_1 Z_1} \tag{3.6}$$

$$= \frac{j100\omega M}{\omega^2 M^2 - \omega^2 L^2 + 2500 + j100\omega L} \tag{3.7}$$

For $\omega \rightarrow 0$,

$$S_{21}(\omega \rightarrow 0) = 0 \tag{3.8}$$

therefore no signal is transmitted to the secondary. while for $\omega \rightarrow \infty$,

$$S_{21}(\omega \rightarrow \infty) \quad = 0 \tag{3.9}$$

thus no transmission because of the infinite impedance in the primary.

S_{11} and S_{21} are plotted in Figure 3.2 on a polar plot. The Smith Chart can be imposed on the polar plot. S_{11} is plotted as a set of red curves that span k from 0 to 1 in steps of 0.1. The arrow in 3.2 indicates the direction where k increases in value. S_{21} is the set plotted in blue curves for the same values of k. and Figure 3.4 presents the S parameter curves on a linear plot. The independent axis is the frequency.

For $k = 0$, there is no coupling between the primary and secondary. The primary by itself is an inductor. The secondary also acts as an inductor. Thus $S_{11} = 1$, and $S_{21} = 0$. Because of symmetry, $S_{22} = 1$, and $S_{12} = 0$.

As k increases, S_{11} starts to decrease at higher frequencies, and then increases again to reach $S_{11}(\omega \rightarrow \infty) = 1$.

As for S_{21}, it increases to a certain value, less than 1, and then decreases till it reaches 0 at ∞. S_{21} takes the shape of a circle that is tangential to 0.

When $k = 1$, complete coupling is achieved between the primary and the secondary. S_{11} starts at $1\angle 180$, and then ends at $S_{11}(\omega \rightarrow \infty) = 0$. S_{21} starts at 0 and $S_{21}(\omega \rightarrow \infty) \rightarrow 1\angle 0$.

In Figure 3.3, as k is swept from 0.8 to 1, it is noted that S_{21} ends in the center of the polar coordinates for $k = 0$ because the structure becomes an inductor and not a transformer anymore.

For $k = 0$, there is no coupling between the primary and the secondary. Therefore $S_{11} = 1$, and $S_{21} = 0$. When k increases, S_{11} decreases, and S_{21} increases. For $k = 1$, $S_{11}(\omega \rightarrow \infty) \rightarrow 0$, and $S_{21}(\omega \rightarrow \infty) \rightarrow 1$.

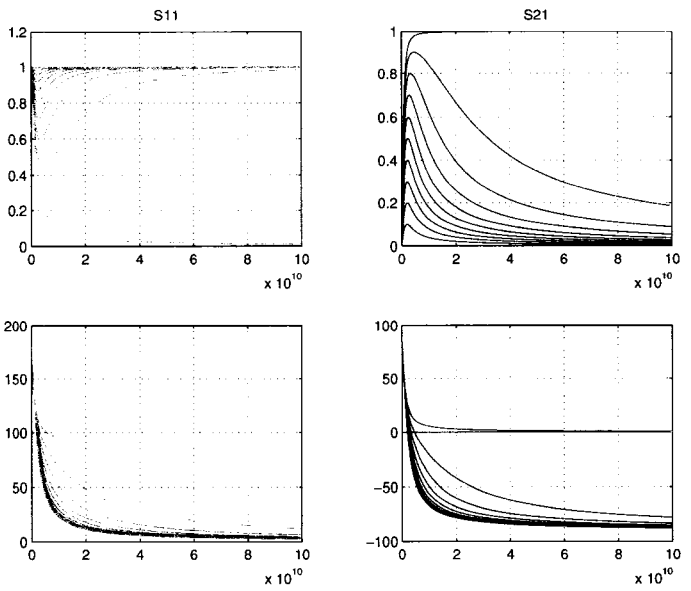

Figure 3.4 S parameters of ideal 2 port transformer on a linear scale

3.2.2 Analysis for ideal four port transformers

Figure 3.5 shows a 4 port ideal transformer subjected to S parameter calculations for S_{11}. The electrical parameters for analysis are listed in Table 3.2. Since this is a 4 port network, 16 S parameters are needed for calculating the complete S parameter matrix.

To calculate S_{11},

$$S_{11} = \frac{V_1 - I_1 Z_1^*}{V_1 + I_1 Z_1} \tag{3.10}$$

where $V_2 = -I_2 Z_2$, $V_3 = -I_3 Z_3$, and $V_4 = -I_4 Z_4$. S_{21} is calculated as

$$S_{21} = \frac{V_2 - I_2 Z_2^*}{V_1 + I_1 Z_1} \tag{3.11}$$

where $V_2 = -I_2 Z_2$, $V_3 = -I_3 Z_3$, and $V_4 = -I_4 Z_4$. S_{14}, is calculated as:

$$S_{14} = \frac{V_1 - I_1 Z_1^*}{V_4 + I_4 Z_4} \tag{3.12}$$

where $V_1 = -I_1 Z_1$, $V_2 = -I_2 Z_2$, and $V_3 = -I_3 Z_3$. Table 3.3 lists the analytical expressions for various S_{ij}, $i = 1 \ldots 4$, and $j = 1 \ldots 4$. Because of symmetry in the ideal structure, only 4 parameters need to be calculated and the rest are deduced from them. Referring to

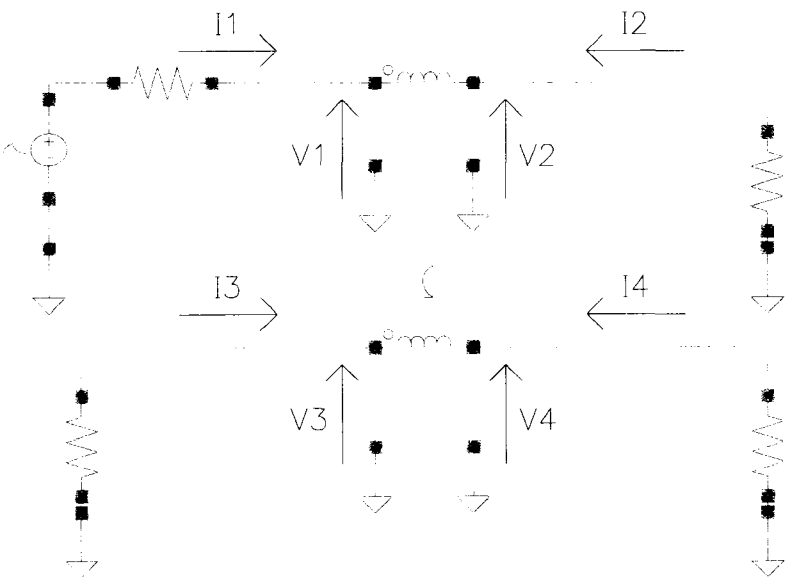

Figure 3.5 Schematic for 4 port ideal transformer

the derivations in section 3.11.2, the differential input to differential output S parameters are shown in Table 3.3.

3.3 Transformer resonance frequencies

The transformer has three (main) resonance frequencies.

1. f_{sp} is the resonance frequency of the primary. This comes from the self-inductance of the primary, and the primary to ground capacitance, and primary to primary capacitances.

2. f_{ss} is the resonance frequency of the secondary. This comes from the self-inductance of the secondary, and the secondary to ground capacitance, and secondary to secondary capacitances.

3. f_c is the coupling resonance frequency. This comes from the inter-winding capacitance between the primary and the secondary.

Other coupling modes may exist because of the inductive and capacitive fringe coupling sets. As for f_{sp} and f_{ss}, a value around 10 GHz is achievable for a planar transformer. The

Table 3.2 Four port ideal transformer parameters

Parameter	Definition
I_1	Current entering the transformer primary (port 1)
I_2	Current entering the transformer primary (port 2)
I_3	Current entering the transformer secondary (port 3)
I_4	Current entering the transformer secondary (port 4)
V_1	Voltage from the transformer primary (port 1) to ground
V_2	Voltage from the transformer primary (port 2) to ground
V_3	Voltage from the transformer secondary (port 3) to ground
V_4	Voltage from the transformer secondary (port 4) to ground
L	Self inductance of the primary or secondary
M	$=k\sqrt{L^2}$. Mutual inductance between the primary and secondary
ω	$=2\pi f$, f is the frequency in Hz

problem is with f_c which can be seen when the transformer 4 port S parameters are converted to 2 port differential input to differential output S parameters. Since a thick metal layer is chosen (Thickness $> 1\mu$m) to achieve high Q, the inter-winding capacitance between the primary and secondary is higher. Therefore, f_c becomes lower. As a result, choosing a thinner lower metal layer increases f_c although the Q factor is lower because of the increase of the series resistance of the primary and secondary windings.

3.4 Effect of changing metal layer

In this section, the effect of changing the metal layer of the transformer is discussed. Changing the metal layer changes the parasitic capacitances of the transformer to the substrate. In effect, the resonance frequencies of the transformer are affected.

Let the design parameters of the transformer be defined as in Table 3.4.

Several transformer structures are simulated in ASITIC. The geometric parameters are listed in Table 3.5. Table 3.6 presents quantitative results regarding the resonance frequencies, and inductance values when the metal layer is changed.

When the layer is increased from M_{thin} to M_{thick}, several characteristics of the transformer are affected accordingly as in Table 3.6. The effects are discussed below:

Table 3.3 Four port ideal transformer S parameters

Parameter	Equation
S_{11}	$=\frac{\omega^2(M^2-L^2)+j100\omega L}{\omega^2(M^2-L^2)+10^4+j200\omega L}$ $=S_{22}=S_{33}=S_{44}$
S_{21}	$=\frac{10^4+j100\omega L}{\omega^2(M^2-L^2)+10^4+j200\omega L}$ $=S_{12}=S_{34}=S_{43}$
S_{31}	$=\frac{j100\omega M}{\omega^2(M^2-L^2)+10^4+j200\omega L}$ $=S_{13}=S_{24}=S_{42}$
S_{41}	$=\frac{-j100\omega M}{\omega^2(M^2-L^2)+10^4+j200\omega L}$ $=S_{14}=S_{23}=S_{32}$
S_{DD11}	$=\frac{\omega^2(M^2-L^2)-10^4}{\omega^2(M^2-L^2)+10^4+j200\omega L}$ $=S_{DD22}$
S_{DD21}	$=\frac{j200\omega M}{\omega^2(M^2-L^2)+10^4+j200\omega L}$ $=S_{DD12}$

1. The self-inductance Lp, Ls(nH) is decreased because the thickness of the metal layer is increased.

2. The mutual inductance Mc(nH), which is a function of Lp, and Ls, is decreased for the same reason in 1.

3. The quality factor Q of the self-inductance increases because increasing the thickness of the metal layer will decrease the effective resistance of the windings. Therefore the loss is reduced.

4. f_s increases as the layer is increased due to the fact that as the winding is placed farther

Table 3.4 Design parameters of the transformer

Parameter	Definition
$Len =$	edge of square that encloses transformer
$W =$	width of interconnect winding
$S =$	spacing between primary and secondary windings
$N =$	number of turns in each of the primary and secondary
$Lp =$	Self inductance of primary
$Ls =$	Self inductance of secondary
$Mc =$	Mutual Inductance between the primary and secondary
$Qp =$	Quality factor of primary alone
$M_{thin} =$	Thickness of thin metal layer $\cong 0.5\mu$m
	M_{thin} is about 4μm above substrate
$M_{thick} =$	Thickness of thick metal layer $\cong 1\mu$m
	M_{thick} is raised 1μm above M_thin

Table 3.5 Transformer geometric parameters

Number	Len	W	S	N	Layer
M_{thin}	260	5	5	3.5	M5
M_{thick}	260	5	5	3.5	M6

away from the substrate, the self-capacitance to substrate is decreased.

5. f_c decreases as the layer is increased because the layer thickness is increased and this, in turn, increases the inter-winding capacitance between the primary and the secondary.

3.5 Objective of research

The objective of the research in this chapter is to design monolithic RF transformers to be part of a high speed data transmission driver, and that have the following properties:

1. Broad Bandwidth to accommodate frequencies up to 5 GHz. In other words, f_{sp}, f_{ss}, and f_c need to be higher than the range of frequencies desired for the operation of the transformer in high frequency applications.

Table 3.6 Increased bandwidth transformer electrical parameters

Number	Lp, Ls (nH)@5GHz	Mc @5GHz	Qp, Qs	f_s GHz	f_c GHz	f_s,est GHz	f_c, est. GHz
TR5	4.89	3.67	2.23	13.94	4.75	11.77	19
TR6	4.84	3.65	6.37	15.04	3.35	11.73	13.4
Layer Inc.	⇓	⇓	⇑	⇑	⇓	⇓	⇓

2. Low loss for a wide band of frequencies of operations.

3. High mutual inductance between primary and secondary in order to induce detectable voltage at the secondary.

The self and coupling resonance frequencies are generally low for the planar transformer. An optimization of the self- resonance frequencies with a high mutual inductance can be achieved but the challenge is in the coupling resonance frequency. It needs to be increased so as to allow frequency components of the signals to be coupled from the primary to the secondary.

3.6 Planar interleaved transformer

In this section, several transformer structures are explored. They are the planar concentric transformer, planar interleaved transformer, and others.

3.6.1 Introduction

The transformer primary and secondary are interleaved in this structure. The input impedance is equal to the output impedance. The coupling coefficient k is high, on the order of 0.8, where

$$k = \frac{M_{12}}{\sqrt{L_1 L_2}} \tag{3.13}$$

where M_{12} is the mutual coupling between the primary and secondary, L_1 and L_2 are the primary and secondary self inductances of the transformer, respectively. The coupling capacitance between the primary and secondary can be relatively high. This is because the primary

or secondary windings are adjacent to each other on both sides except in the outer layer. For example, a primary winding lies between two secondary windings, and vice versa.

This increased coupling capacitance with the increased mutual inductance M between the primary and secondary, results in a reduced coupling resonance frequency. This means that the transformer stops acting like a transformer after a certain frequency $f_{c,res}$.

$$f_c = \frac{1}{2\pi\sqrt{C_c M_{12}}} \tag{3.14}$$

where C_c is the coupling capacitance between the primary and secondary windings in the same layer. Fringing capacitance can be added to the parallel plate capacitance to give a better approximation. A photomicrograph of the interleaved transformer in a 0.18μm CMOS process is shown in Figure 3.6.

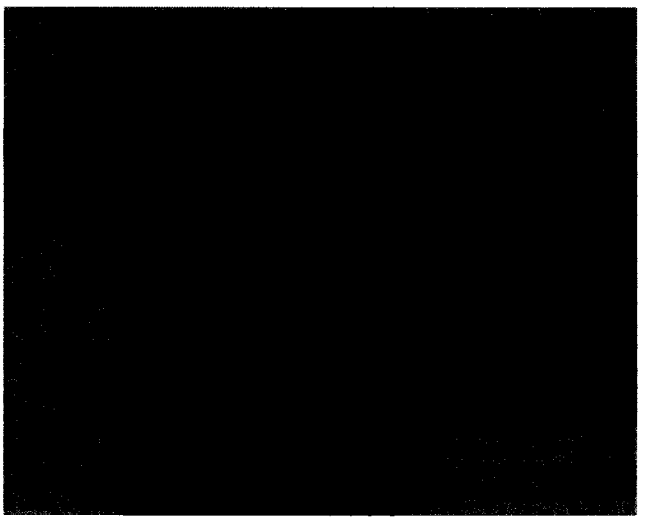

Figure 3.6 Chip photomicrograph of planar interleaved windings with no shield in thick metal layer

3.6.2 Bandwidth improvement of planar interleaved transformer

The coupling resonance frequency f_c is directly related to the mutual side capacitance between the primary and the secondary windings. In addition, f_c is also related to the mutual inductance between the primary and the secondary. Note that the capacitance affects mainly two windings: the ones adjacent to each other. On the other hand, the mutual inductance

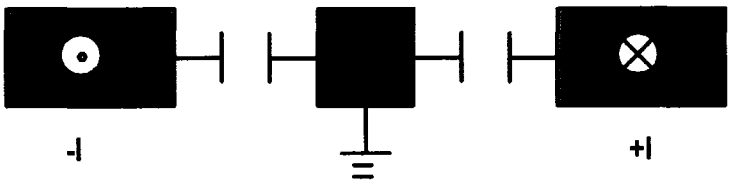

Figure 3.7 Coupling capacitance converted to substrate in planar interleaved transformer

affects more than the winding directly adjacent to the original winding. This shielding feature can be utilized to increase f_c. One way to do that is to introduce a shield that is placed between the primary and the secondary. This shield hides the primary from the secondary capacitively but not inductively [49]. As a result, the capacitance from primary to secondary is converted to two equal capacitances from primary to shield and from secondary to shield. If the shield is grounded to substrate, then the primary-secondary coupling capacitance is converted to primary to ground and secondary to ground self-capacitance as shown in Figure 3.7. It should be noted that the shield becomes more effective in shielding the magnetic field when the frequency increases due to the reduction in the skin depth. Therefore at higher frequencies, the mutual inductance might be affected.

As a result, the coupling bandwidth of the planar Interleaved transformer can be improved by adding, in the same metal layer, a thin metal shield between the primary and the secondary. The shield should be the minimum width that can withstand a via connected to it. This shield is connected to ground or substrate. The shield eliminates most of the coupling capacitance, C_c between the primary and secondary. Therefore, C_c is decreased to just the fringing capacitance between the primary and secondary, while the primary self capacitance, C_{sp}, and secondary self capacitance, C_{ss}, each is increased by $2C_c$.

This has the effect of increasing f_c, while f_{sp}, and f_{ss} are decreased. It is important to make the shield as thin as possible so that the increase in C_{sp}, and C_{ss} is minimal and the reduction in f_{sp} f_{ss} is minimal too. The shield should not be continuous between the primary and the secondary, and should be segmented into short segments in order to prevent any induced currents in it.

Consequently, when converting the coupling capacitance to a self-capacitance at the primary and secondary, the self-resonance frequency is affected. The following example estimates the decrease in f_{sp} and f_{ss}.

Example: let the spacing between primary and secondary be S, and $S = H$ where H is the distance between the winding and the substrate. The capacitance of the winding to the substrate is around $C_{sp}/m = \varepsilon W/H$. Then, $f_{sp} = 1/2\pi\sqrt{LC_{sp}}$. If a shield is introduced between the primary and the secondary then the capacitance from primary to shield, and from secondary to shield is $C_c/m \cong 2\varepsilon t/S$ for each winding where t is the thickness of the metal layer. Since the winding has coupling capacitance to ground on both sides, the total coupling capacitance, $C_{ctot}/m \cong 4\varepsilon t/S$. Assuming $t = 0.1W$, where W is the winding width, then $C_{ctot}/m \cong 0.4\varepsilon W/H$. As a result, the new resonance frequency can be written as:

$$\begin{aligned} f_{p,est} &= \frac{1}{2\pi\sqrt{L\left(C_p + C_{cptot}\right)}} \\ &= \frac{1}{2\pi\sqrt{L\left(1.4C_p\right)}} \\ &= \frac{0.845}{2\pi\sqrt{L\left(C_p\right)}} \end{aligned}$$

In general, it can be shown that $f_{sp,est} = f_p/\sqrt{1 + 4t/W}$. Therefore, as t decreases, and W increases, this equation gives an approximation of the new resonance frequency due to the shield effect. Please see Table 3.6 for the modified self-resonance frequencies. As for f_c, it increases considerably because the coupling capacitance is reduced to a fringing factor that might be a small fraction of the original capacitance (approximately 1/4 of the original capacitance. Therefore, $f_{c,est}$ can be several times the original f_c; around 4 times.

3.6.3 Layout consideration of the transformer

The proposed layout for the transformer can be seen in Figure 3.8. The shield consists of a series of metal strips that are placed between the primary and secondary windings. Each shield segment is connected through a set of vias to the substrate. The substrate is grounded by connecting the pads to substrate and by having down-bonding pads to the back of the chip.

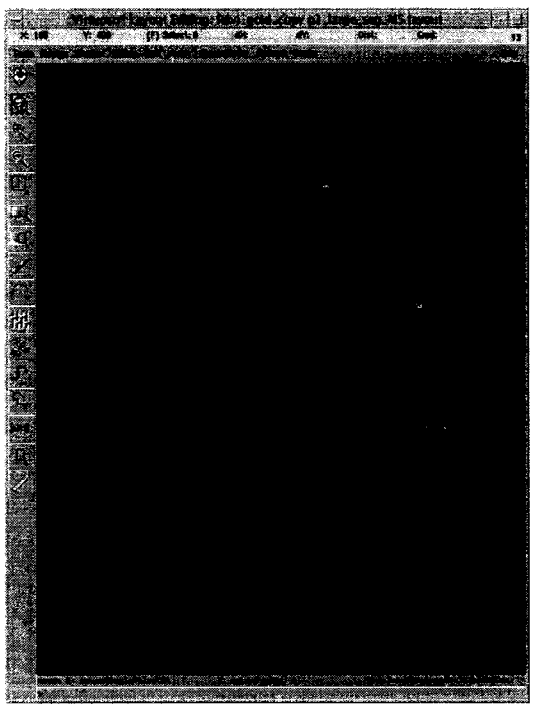

Figure 3.8 Layout of the transformer windings with long shields in *Cadence*®

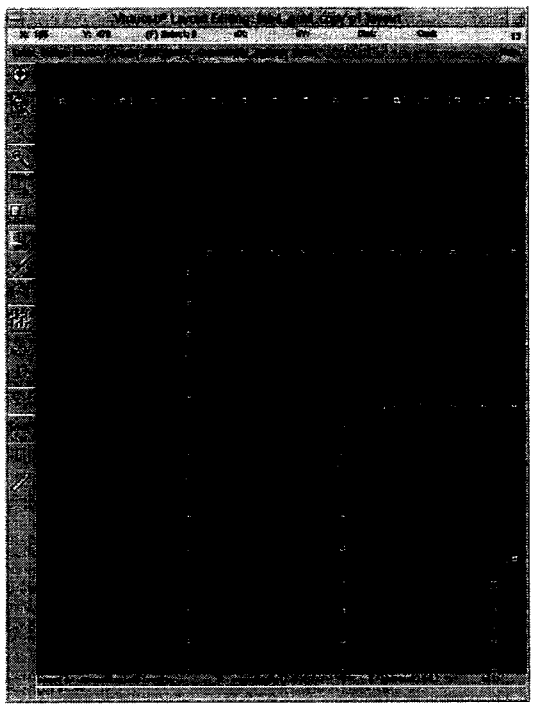

Figure 3.9 Layout of the transformer windings with short shields in *Cadence*®

Two variations of shields were implemented. Figure 3.8 shows small shield segments and Figure 3.9 shows long shield segments connected at only one point for each edge of the windings.

A better way to place the shield as a "wall" between the primary and secondary. The wall starts from the substrate, and extends above the layer where the transformer exists. The shield eliminates the fringe capacitance between the primary and secondary. However, there exist some processing challenges making such "wall". Metal spikes may develop into the substrate if the vias are too large or wide.

The shield between the primary and secondary of the transformer may serve as shield for a surge in voltage that is imposed on the primary of the transformer. This structure can be considered as a secondary protection measure against an ESD event.

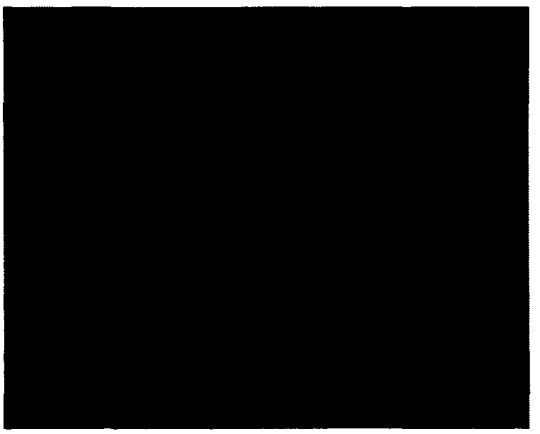

Figure 3.10 Chip photomicrograph of the transformer with long shields

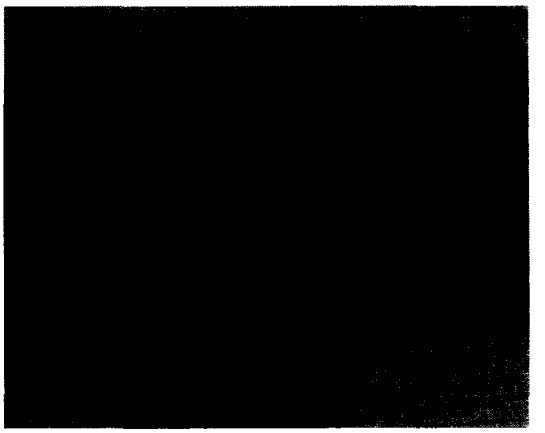

Figure 3.11 Chip photomicrograph of the transformer with long shields *(zoom in)*

3.7 Planar concentric transformers

The transformer structures are laid out as the whole primary winding in the center and the whole secondary winding around it. the primary can be interchanged with the secondary. The structure is obviously not symmetric, and the the coupling coefficient is lower than the case for the Interleaved Transformer because the windings are farther away from each other. This means that a considerable amount of the signal won't be transmitted from the primary to the secondary. The self capacitances C_{sp}, and C_{ss} can be close to each other by optimizing the area each winding occupies.

3.7.1 Bandwidth improvement of planar concentric transformers

The structure inherently has a lower C_{cp} than the interleaved case because the coupling capacitance is seen between only the outer edge of the last winding of the inner windings and the inner edge of the first winding of the outer winding. Therefore $f_{c,res}$ of this winding can be higher than in the Interleaved case. The $f_{c,res}$ can be maximized by using a shield between the primary and secondary winding as in the first case.

3.8 Planar ring transformers

Other transformer structures were studied beside the aforementioned fabricated designs above. In the beginning, an inductor structure is designed. Then, the inductor structure can be expanded to be a transformer. One inductor design for a transformer is to make the transformer in the form of two rings. The flux lines are perpendicular to the rings. The winding is made such that the current lows in one of the rings clockwise. In the other ring, the current flows in the counter clockwise direction. If the flux leaves one of the rings then it enters the other ring. The ring area of one of the rings is made equal to the area of the other. The flux flows from one of the rings to the other. A sample inductor with one winding per ring is shown in Figure 3.12. The inner ring is marked by the blue color, while the outer ring is marked by the brass color. Please note that the blue and brass color rings are virtual and not physical geometries.

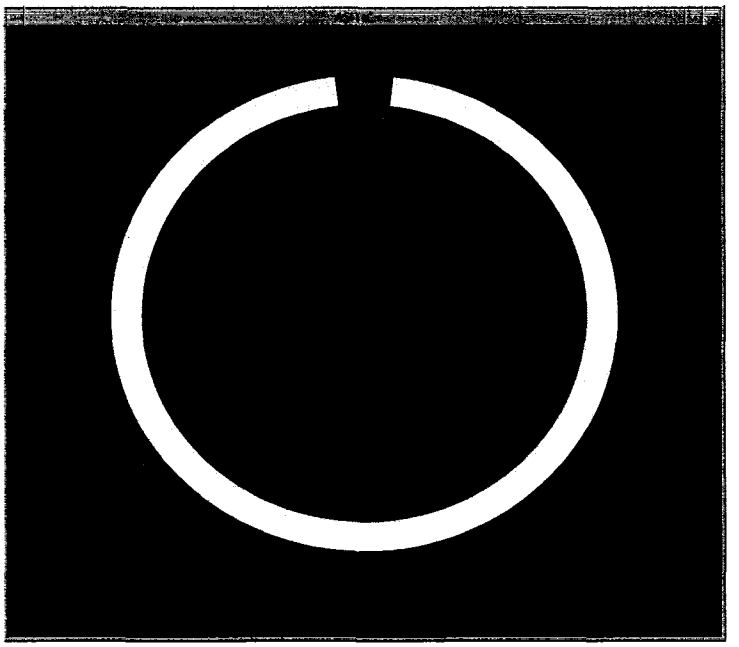

Figure 3.12 Two ring transformer layout

Previous work on this design is in [21] where the flux flows from one winding of the inductor to another. The flow of flux from one inductor to the other is just in one direction. However,

in the case of the ring inductor, the outside ring encircles the inner ring from all directions as in Figure 3.12. As in [21], horizontal guides for the flux can be added in the form of rings between the aforementioned rings. These *guide rings* should be located on top of the inductor plane and underneath the inductor plane. The number of rings on top and bottom can be reduced by having the rings farther away from the inductor layer. As a result, the inter-layer dielectric thickness can be high.

The extension of this inductor design to a transformer design can be done by adding winding rings inside the planar inductor which becomes now, say, the primary. The new rings become the secondary.

3.9 Design of planar transformers using ASITIC and MATLAB interface

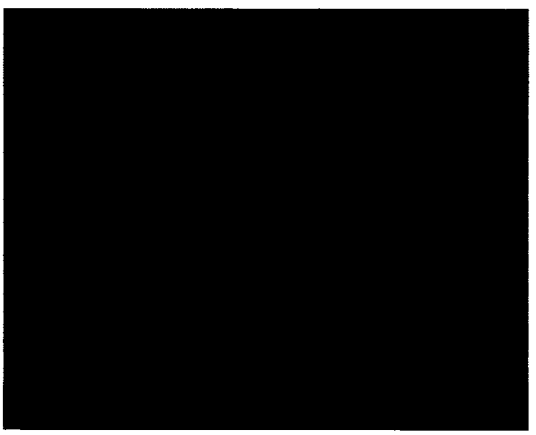

Figure 3.13 Chip photomicrograph of the transformer with short shields

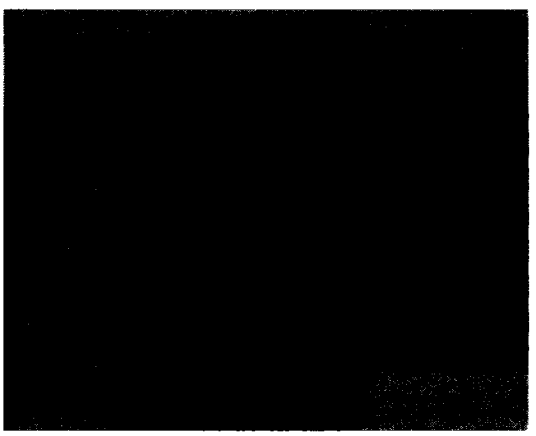

Figure 3.14 Chip photomicrograph of the transformer with short shields *(zoom in)*

A MATLAB interface was developed for designing transformers in ASITIC. For complex transformer structures, it is difficult to generate ASITIC input files by hand. In addition, if a sweep of a parameter, or an optimization of a parameter is desired, this interface is helpful in performing these tasks.

The interface makes it easier to automatically generate ASITIC input files. ASITIC uses these input files to generate the transformer geometric model and performs simulations on it

to get electrical parameters such as resonance frequencies, quality factor, parasitic resistances and capacitances, and scattering parameters. The software interface receives the simulation results from ASITIC and analyzes the data for all the simulation runs. The results can be plotted in MATLAB. This interface contributes to the design of RF transformers within the design constraints.

Several versions of the interface are developed. They are customized for the type of parameter sweep required. The interface code is listed in Appendix A.

3.10 Transformer structures fabrication in a 0.18μm CMOS process

Several transformer structures were fabricated in a 0.18μ CMOS process. The structures include 3 port and 4 port transformers. The 4 port structures include a regular planar interleaved transformer, bandwidth improved transformer with short shields, and with long shields.

For each port of the transformer, there exist three pads compatible with the Ground-Signal-Ground microwave probe tips used later in testing. The signal pad connects the RF element port to the middle probe tip. The two remaining ground pads connect the two edge probe tips to the ground substrate. Pads connect the substrate to the signal pad and are located at four corners of the structure. In this way, the substrate can be connected to the shield layer, or the substrate can be connected separately. Additional substrate pads are located at the corners of the chip. These pads are connected to the paddle under the chip. This allows for substrate grounding while testing.

The transformer element core area is $260\mu\text{m}\times260\mu\text{m}$. As for the pads, for each port there needs to be a set of three pads aligned together. The pads are $75\mu\text{m}\times75\mu\text{m}$ each with spacing between pads inner edges of 25μm. These dimensions are compatible with the test probe tips. Note that the sets of pads form a square like shape on the periphery of the transformer. It was also taken into consideration that the pads are placed in way that would let the four microwave probe tips be placed on the transformer structure simultaneously.

3.11 Four port RF transformer test procedure

The S parameters of the 4-port transformers were extracted using an HP 50 GHz Network Analyzer. One issue in measurement is in calibrating the 4 probe tips simultaneously. Two of the probe tips are connected to the network analyzer and are calibrated. The other 2 probe tips are terminated in 50Ω. The measurement assumes that the probe tips are calibrated to 50Ω. In reality, these probe tips use are terminated without calibration to 50Ω.

The other difficulty in measurement is the parasitic effect of the pads that is present in the S parameters. Therefore the pad parasitic effect needs to be reversed in the S parameter set. This can be performed by the pad de-embedding method.

Recalibration is performed by converting S parameters to T parameters and then performing probe recalibration as in Section 3.11.1[67]. Parasitic pad de-embedding is performed by converting the S parameters to Y parameters and then de-embedding the pad parasitics as in Scction 3.11.2.

3.11.1 S parameters probe recalibration using a T transformation

The test procedure uses 4 microwave test probes and tips. Six S parameters readings are taken. They are:

1- From Port 1 to port 2 while Ports 3 and 4 are terminated with 50Ω.

2- From Port 1 to port 3 while Ports 2 and 4 are terminated with 50Ω.

3- From Port 1 to port 4 while Ports 2 and 3 are terminated with 50Ω.

4- From Port 2 to port 3 while Ports 1 and 4 are terminated with 50Ω.

5- From Port 2 to port 4 while Ports 1 and 3 are terminated with 50Ω.

6- From Port 3 to port 4 while Ports 1 and 2 are terminated with 50Ω.

Ports 1, and 2 are calibrated by the network analyzer. Re-calibration for ports 3 and 4 is made because these ports are replaced during measurements. They are measured for open, short and through connections. The third probe recalibration S parameters matrices, are:

$$S_{11}^{Port3} = \Gamma_{short}^{Port3} \tag{3.15}$$

$$S_{22}^{Port3} = \frac{2\Gamma_{short}^{Port3} - (S_{11}^{Port3} + \Gamma_{open}^{Port3})}{\Gamma_{short}^{Port3} - \Gamma_{open}^{Port3}} \tag{3.16}$$

$$S_{21}^{Port3} = \sqrt{S_{11}^{Port3} S_{22}^{Port3} - \Delta_s} \tag{3.17}$$

$$S_{21}^{Port3} = S_{12}^{Port3} \tag{3.18}$$

where $\Delta_s = S_{11}S_{22} - S_{21}S_{12}$, while the forth probe re-calibration parameters are:

$$S_{11}^{Port4} = \Gamma_{short}^{Port4} \tag{3.19}$$

$$S_{22}^{Port4} = \frac{2\Gamma_{short}^{Port4} - (S_{11}^{Port4} + \Gamma_{open}^{Port4})}{\Gamma_{short}^{Port4} - \Gamma_{open}^{Port4}} \tag{3.20}$$

$$S_{21}^{Port4} = \sqrt{S_{11}^{Port4} S_{22}^{Port4} - \Delta_s} \tag{3.21}$$

$$S_{21}^{Port4} = S_{12}^{Port4} \tag{3.22}$$

The 4 Port S parameter matrix of the coupled transformer, can be written as:

$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} = \begin{bmatrix} S_{11}^{Port1,2} & S_{12}^{Port1,2} & S_{12}^{Port1,3} & S_{12}^{Port1,4} \\ S_{21}^{Port1,2} & S_{22}^{Port1,2} & S_{12}^{Port2,3} & S_{12}^{Port4,2} \\ S_{21}^{Port1,3} & S_{21}^{Port2,3} & S_{22}^{Port1,3} & S_{12}^{Port4,3} \\ S_{21}^{Port1,4} & S_{21}^{Port4,2} & S_{21}^{Port4,3} & S_{22}^{Port1,4} \end{bmatrix} \tag{3.23}$$

Defining the T-parameters matrix as:

$$\begin{bmatrix} T \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \tag{3.24}$$

The S-parameters matrix is transformed to T-parameters matrix using:

$$T_{11} = -\frac{\Delta_s}{S_{21}} \tag{3.25}$$

$$T_{12} = \frac{S_{11}}{S_{21}} \tag{3.26}$$

$$T_{21} = \frac{S_{22}}{S_{21}} \tag{3.27}$$

$$T_{22} = \frac{1}{S_{21}} \tag{3.28}$$

For each of the six measurements, there is a specific S to T transformation matrix to recalibrate for port 3 and port 4.

$$\begin{bmatrix} T \end{bmatrix}_{Port1,2}^{recal} = \begin{bmatrix} T \end{bmatrix}_{Port1,2}^{uncal} \tag{3.29}$$

$$\left[\ T\ \right]^{recal}_{Port1,3} = \left[\ T\ \right]^{uncal}_{Port1,3} \left[\ T\ \right]^{-1}_{Port3} \tag{3.30}$$

$$\left[\ T\ \right]^{recal}_{Port1,4} = \left[\ T\ \right]^{uncal}_{Port1,4} \left[\ T\ \right]^{-1}_{Port4} \tag{3.31}$$

$$\left[\ T\ \right]^{recal}_{Port2,3} = \left[\ T\ \right]^{uncal}_{Port2,3} \left[\ T\ \right]^{-1}_{Port3} \tag{3.32}$$

$$\left[\ T\ \right]^{recal}_{Port4,2} = \left[\ T\ \right]^{-1}_{Port4} \left[\ T\ \right]^{uncal}_{Port4,2} \tag{3.33}$$

$$\left[\ T\ \right]^{recal}_{Port4,3} = \left[\ T\ \right]^{-1}_{Port4} \left[\ T\ \right]^{uncal}_{Port4,3} \left[\ T\ \right]^{-1}_{Port3} \tag{3.34}$$

For each re-calibrated T transformation, the T to S transformation is performed again where

$$\left[\ S\ \right] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{3.35}$$

and

$$S_{11} = \frac{T_{12}}{T_{22}} \tag{3.36}$$

$$S_{12} = \frac{\Delta_T}{T_{22}} \tag{3.37}$$

$$S_{21} = \frac{1}{T_{22}} \tag{3.38}$$

$$S_{22} = -\frac{\Delta_T}{T_{21}} \tag{3.39}$$

3.11.2 S parameters pad parasitic decoupling using a Y transformation

In this subsection, the objective is to obtain the de-embedded S parameters of the transformer. The S-parameters matrix is transformed to Y-parameters matrix using:

$$Y_{11}^{dec} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_o \tag{3.40}$$

$$Y_{12}^{dec} = \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_o \tag{3.41}$$

$$Y_{21}^{dec} = \frac{-S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_o \tag{3.42}$$

$$Y_{22}^{dec} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_o \tag{3.43}$$

where $Y_o = 1/50$. The de-embedded Y parameters are converted back to S parameters through:

$$S_{11}^{dec} = \frac{(Y_o - Y_{11})(Y_o + Y_{22}) + Y_{12}Y_{21}}{(Y_o + Y_{11})(Y_o + Y_{22}) - Y_{12}Y_{21}} \tag{3.44}$$

$$S_{12}^{dec} = \frac{-2Y_{12}Y_o}{(Y_o + Y_{11})(Y_o + Y_{22}) - Y_{12}Y_{21}} \tag{3.45}$$

$$S_{21}^{dec} = \frac{-2Y_{21}Y_o}{(Y_o + Y_{11})(Y_o + Y_{22}) - Y_{12}Y_{21}} \tag{3.46}$$

$$S_{22}^{dec} = \frac{(Y_o + Y_{11})(Y_o - Y_{22}) + Y_{12}Y_{21}}{(Y_o + Y_{11})(Y_o + Y_{22}) - Y_{12}Y_{21}} \tag{3.47}$$

The 4 port S-parameter matrices are transformed to 2 port differential input to differential output S parameters by using the relations:

$$S_{11}^{DD} = (S_{11} - S_{13} - S_{31} + S_{33})/2 \tag{3.48}$$

$$S_{12}^{DD} = (S_{12} - S_{32} - S_{14} + S_{34})/2 \tag{3.49}$$

$$S_{21}^{DD} = (S_{21} - S_{41} - S_{23} + S_{43})/2 \tag{3.50}$$

$$S_{22}^{DD} = (S_{22} - S_{42} - S_{24} + S_{44})/2 \tag{3.51}$$

The common mode to differential mode S parameters are calculated using:

$$S_{11}^{CD} = (S_{11} + S_{13} + S_{31} + S_{33})/2 \tag{3.52}$$

$$S_{12}^{CD} = (S_{12} + S_{32} + S_{14} + S_{34})/2 \tag{3.53}$$

$$S_{21}^{CD} = (S_{21} + S_{41} + S_{23} + S_{43})/2 \tag{3.54}$$

$$S_{22}^{CD} = (S_{22} + S_{42} + S_{24} + S_{44})/2 \tag{3.55}$$

These parameters describe the behavior of the transformer as a function of frequency. From this data a broadband model of the transformer can be generated using an optimization method. The S parameter set can be directly used as a four port device in *Spectre*®.

3.11.3 Common Mode Rejection Ratio calculations

The Common Mode Rejection Ratio (CMRR) is an indication of how the common mode at the primary of the transformer is rejected at the secondary. There are several definitions for the CMRR. They depend on the number input ports and output ports. One definition is about a single input to differential output. The definition described here is for a network with 2 input ports and 2 output ports. In [55], [19], [45] and [24], the CMRR is the ratio

of the differential input to differential output gain G_{DD}, to the common mode input gain to differential output gain G_{CD}. Therefore, the expression used in analysis here is:

$$CMRR = \frac{S_{21}^{DD}}{S_{21}^{CD}} \tag{3.56}$$

3.12 Transformer characterization results in a 0.18μ CMOS process

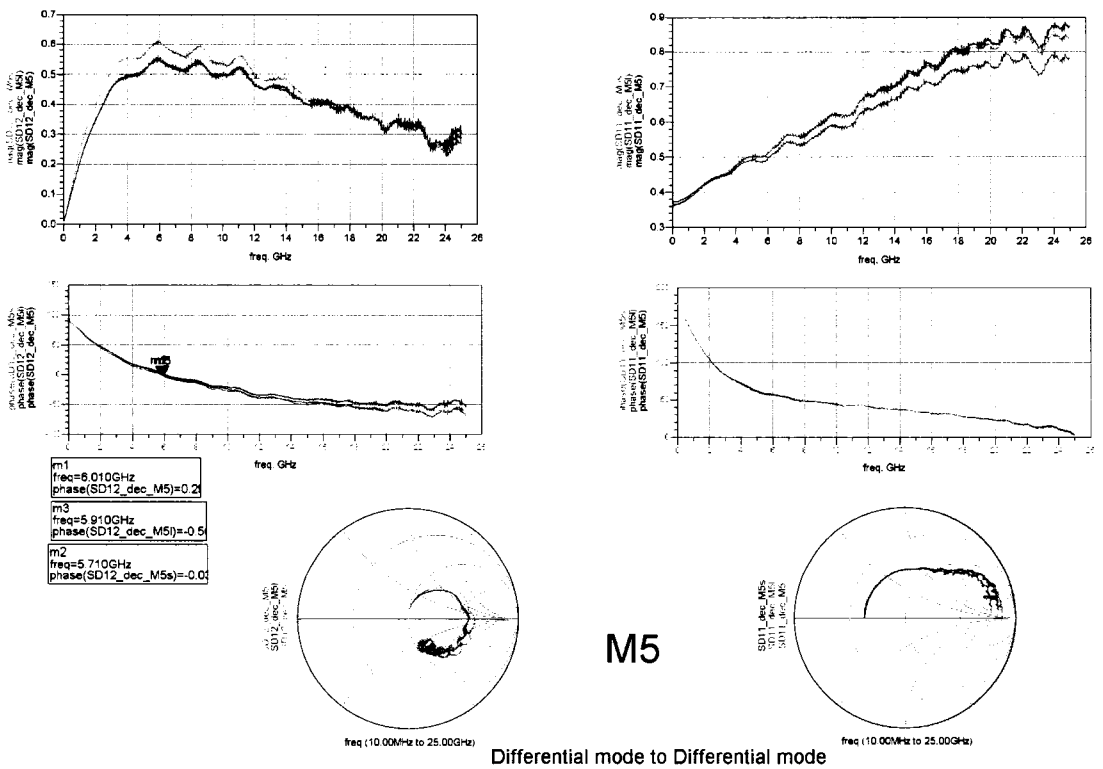

Figure 3.15 S_{DD} of the transformer in thin metal layer

Characterization results for the planar interleaved transformers are discussed in this section. The chip substrate is non-epitaxial with high resistivity on the order of several tens of Ω·cm. Simulation results for the transformers are presented.

Figure 3.15 presents S_{DD} of the transformers (no shields, with short shields, and with long shields). The top linear graphs on the left side present S_{DD12} with phase in degrees. f_c was shown to be as in Figure 3.15 for no shields, short shields and long shields to be 6.01GHz,

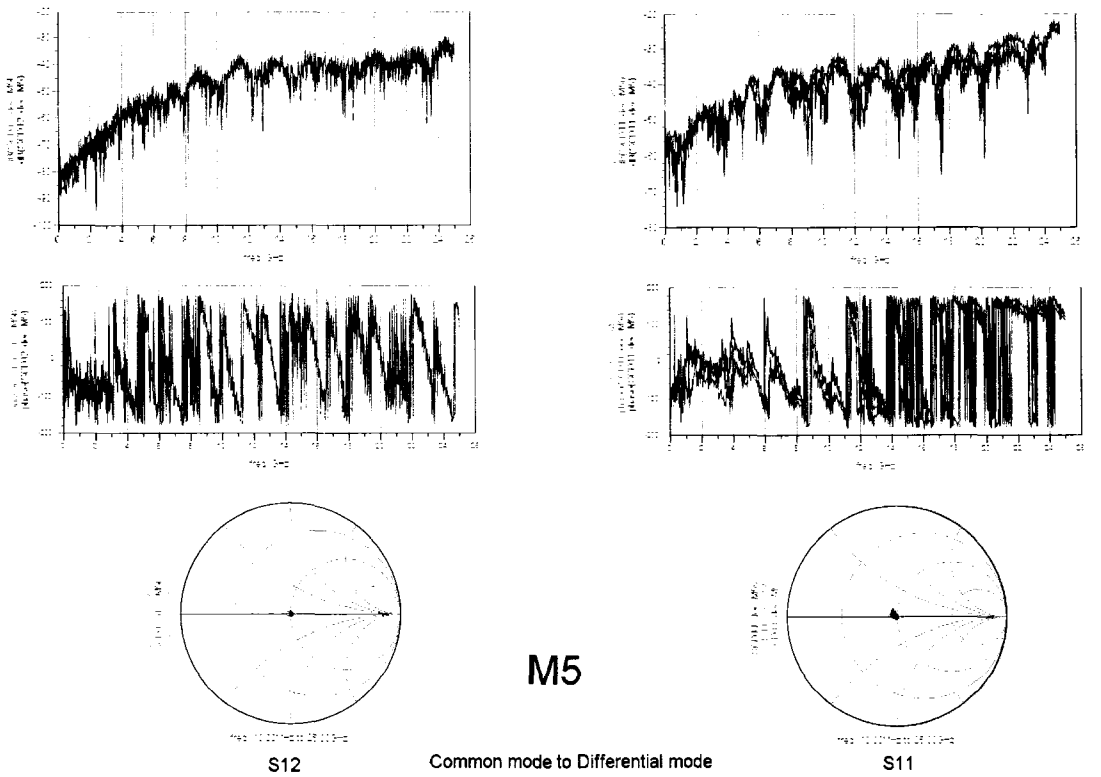

Figure 3.16 S_{CD} of the transformer in thin metal layer

5.71GHz, and 5.9GHz respectively. The resonance frequencies are comparable to each other. There was no significant increase in f_c when the shield is introduced.

The substrate used is high impedance. The shields need to be grounded to the ground pads not through the substrate but through direct metal contact to the ground pads. The metal contact between the shield elements and the ground pad is not present in this fabrication run.

The top linear graphs on the right side of Figure 3.15 represent the magnitude and phase of S_{11} which increases with frequency.

The Smith Chart on the left of Figure 3.15 represents S_{21} which starts at $S_{21}(\omega = 0) = 0$. The structure follows a similar path to S_{21} in Figure 3.2. Because of the parasitic capacitances and resistances, and the nature of the structure, $k < 1$.

The Smith Chart on the right represents S_{11}. Because of the series resistance of the windings, S_{11} starts around 0.36 instead of 0. The S_{11} curves deviate from the ideal case in

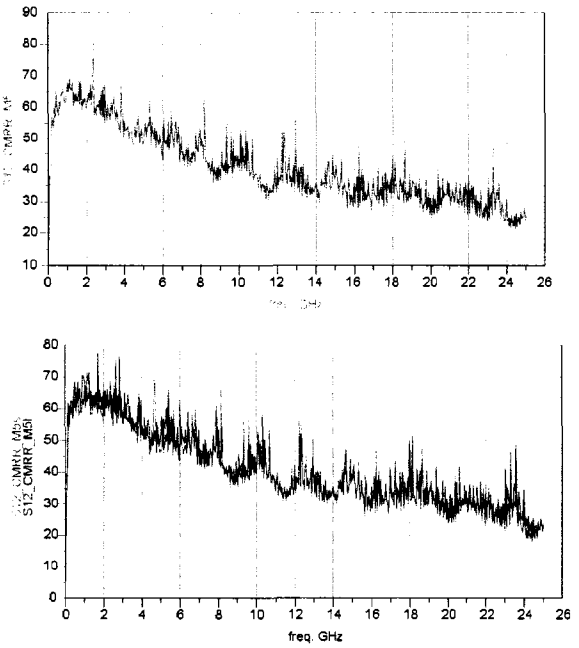

Figure 3.17 $CMRR$ of the transformer in thin metal layer

Figure 3.2 because of the parasitics at high frequencies.

Figure 3.16 presents S_{CD} of the transformer. The graphs on the left show S_{CD12}. Up to f_c = 6GHz, $S_{CD12} < -45$dB. The graphs on right show S_{CD11}. $S_{CD12} < -35$dB up to f_c = 6GHz. The $CMRR$ is plotted in Figure 3.17. $CMRR > 45$dB up to 6GHz.

3.13 Contribution summary

The contribution of this chapter is the analysis, design, fabrication and characterization of monolithic RF transformers in a 0.18μm CMOS process. Analysis is provided for 4 port ideal transformers. Several transformer structures ar discussed such as planar interleaved transformers and proposed layout changes that have the potential in increasing the transformer coupling bandwidth. A ring transformer structure is introduced that allows less eddy current loss being introduced into the substrate. A software interface is developed in MATLAB, for helping in designing transformer in ASITIC. Recalibration and decoupling methods are

presented too. Characterization results of the RF transformers agree with the design objective presented in this chapter. The resonance frequencies 6 GHz of the transformer are higher than the bandwidth required 5 GHz.

CHAPTER 4. Bandwidth improvement of toroidal transformers

4.1 Introduction

Transformers (TR) are vital elements in this project. They have several responsibilities. They act as an interface between the transmitter chip and the PCB interconnections. Also, they act as a protection device for the chip. Since digital data is transmitted through the TR to the PCB MSL, the transformer needs to be capable of passing a wider range of frequency contents of the signal as opposed to typical microwave TR's which pass a narrow band of frequencies and need to have a high quality factor. There are several monolithic planar transformer structures that exist. A specific type of transformers called toroidal solenoids is discussed in this chapter.

The simulation software used in this project is mainly ASITIC. MATLAB custom programs were also written to calculate the resonance frequencies of the transformer.

4.2 Simulation and design using ASITIC

ASITIC [44] is a free simulation tool for RF transformers and inductors. It offers high frequency simulation capabilities. In the author's opinion, it is more user-friendly than FastHenry [32] and it was developed to handle planar structures in a silicon process. In addition, it can produce a layout structure compatible with silicon layout CAD tools.

In this project, a MATLAB interface was developed in order to sweep the design parameter space for the transformer in order to choose the best performance parameters in terms of resonance frequency, scattering parameters, quality factor, and minimum area size. This MATLAB interface can be easily modified to include an optimization algorithm to find an optimized design.

4.3 Description of toroidal solenoid transformers

Toroidal solenoid transformers are usually built off chip on a ferrite core. Some applications are found in the power electronics field as in [42], and [22]. The magnetic flux flows in the core in a loop. Therefore the flux is contained in that volume. The toroidal solenoid implementation faces several challenges on chip.

There are several publications in the literature about RF toroidal solenoidal inductors and transformers. In [68], the inductor is micro-machined to generate the solenoid. In [35], an air gap is made underneath the inductor to reduce the parasitic capacitance to the substrate. In both designs, the via is large since it does not follow the standard small via size rule. This procedure reduces the series resistance of the toroid and thus improves the quality factor. The inductor toroid can be wound on a cube as in [70]. The height of the cube is 500μm. The toroid cube is mount on the substrate and can be connected to circuit elements on chip. In another implementation, a magnctic core can be fabricated to be inside the the core of the inductor as in [39]. The inductor operating range is within several MHz. A similar approach where a magnetic core is fabricated inside the coil is cited in [1] with a frequency range in KHz range. In [37], a solenoid is made by using a thick dielectric layer of 12μm between the top and bottom layers. In [71], the solenoid is made in a thick film process.

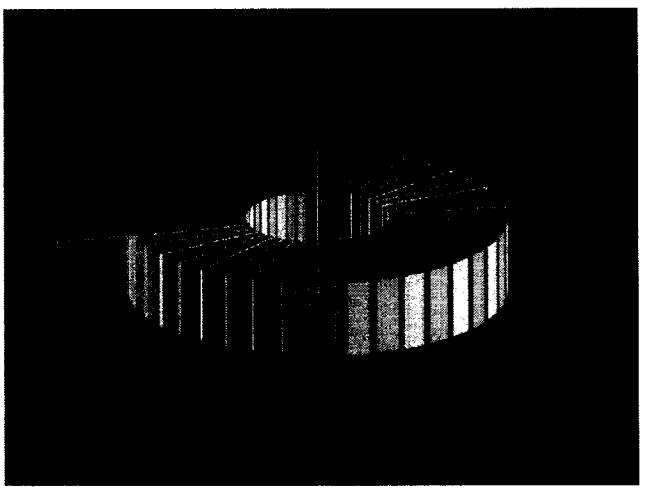

Figure 4.1 3D view of toroidal transformer

A 3D view of one implementation of the toroidal transformer is shown in Figure 4.1, where the lower layer is always different from the top layer. This means that if the top layer is the primary, then the bottom layer is the secondary. A top view is shown in Figure 4.2. The complete via connection between layers is not illustrated.

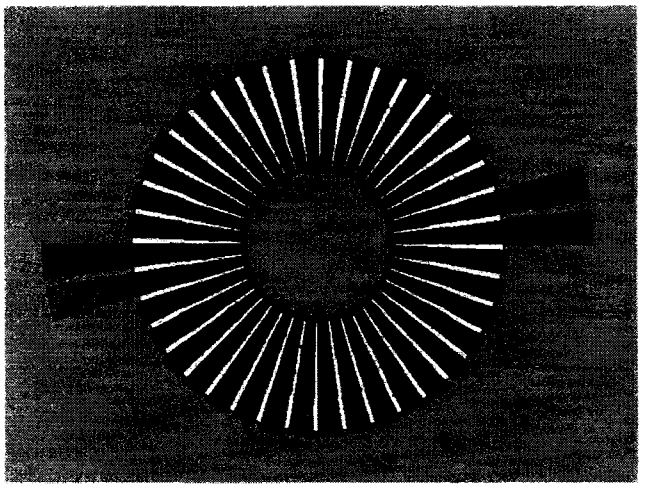

Figure 4.2 Top view of toroidal transformer

4.4 Merits of toroidal solenoidal transformers

There are several merits in toroidal transformer design for high frequency circuits. In the planar spiral transformer structure, the magnetic flux generated by the primary windings is perpendicular to the plane of the transformer and penetrates the chip substrate. The penetrating flux can generate eddy currents in the substrate. Sensitive circuits close to the transformer can be affected by the transformer flux and this can increase the noise floor in the victim circuit and can complicate the design.

The toroidal solenoid on the other hand, has the flux flowing inside the transformer loops and circulating in a loop that takes a ring shape. The flux is contained inside the toroidal solenoid. Only flux leakage penetrates into the substrate and thus noise affects other sensitive circuits from the toroidal transformer is much less than the case of a spiral interleaved transformer. Therefore, it can be a very good candidate for very high frequency applications where

noise is an issue.

4.5 Geometrical model of the toroidal solenoid

The toroidal solenoid was built using MATLAB. MATLAB generates the ASITIC input file. This file was used to generate the toroidal solenoid layout. The layout is displayed in ASITIC as shown in Figure 4.3 and then saved in CIF format. This can be imported into Cadence's layout tool to prepare for fabrication. The script file is listed in Appendix B.1

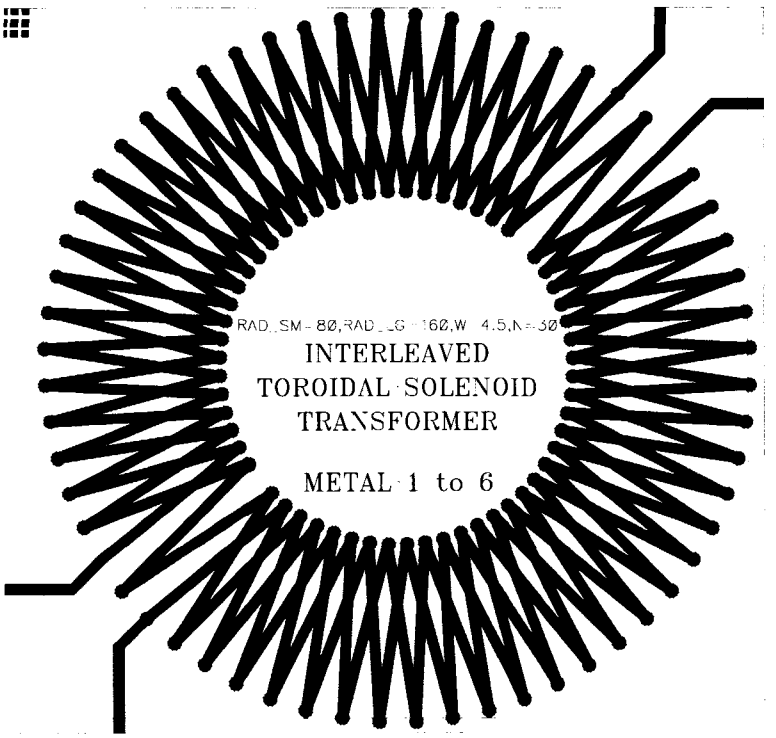

Figure 4.3 Toroidal solenoid transformer generated in MATLAB and ASITIC

An interleaved winding approach is cited to have better coupling between primary and secondary [50]. The winding method is chosen to be the interleaving of primary and secondary windings together around a dielectric core.

4.6 Electrical model of a toroidal transformer

In order to achieve higher inductance, the cross-section of the toroid should have a considerable height. The standard CMOS 0.18μ process has an oxide thickness of less than 5μm between the lowest metal layer and the highest one. In order to achieve a larger loop area for the winding, more windings should be made in the toroid. Unfortunately, this leads to an increase in the self capacitance to ground of the primary and secondary. The problem of oxide thickness can be approached by increasing the oxide thickness in a custom process. In this way, a lower number of windings is needed to form the toroidal solenoid coil, and the self capacitance of the primary and secondary is decreased.

The second problem is the coupling capacitance between the primary and the secondary. Two factors contribute to the coupling capacitance. The first factor comes from the interwinding capacitance between the primary and the secondary winding segments in the same metal layer. This is called side capacitance. The other coupling factor comes from the interwinding capacitance between the primary and secondary overlapping vertically when one conductor segment is at the higher metal layer and the other is in the lower metal layer capacitance. This is called top-bottom layer. The contribution of this factor to the total coupling capacitance can be high.

There are several variations of monolithic toroidal solenoid structures. In this section, a quantitative analysis of a specific monolithic toroidal transformer structure is provided. The toroidal structure assumes an overall circular shape. A top view of the toroidal transformer is shown in Figure 4.3. The primary winding terminals are shown at the lower left corner. The secondary windings terminals are at the upper right corner.

4.6.1 Definitions

The geometric parameters related to the toroidal structure are defined in Table 4.1:

It can be shown that

$$2\pi r_m = (N_p + N_s)\oslash_{pm} + (N_p + N_s)\oslash_{sp} \tag{4.1}$$

Table 4.1 Definitions for a toroidal solenoid geometrical model

Parameter	Description
r_a	inner radius
r_b	outer radius
$r_m = \left(\frac{r_a + r_b}{2}\right)$	middle radius
$l = 2\pi r_m$	Perimeter of the middle ring
W	Width of winding
A	cross section area of toroid loop
N_p	number of turns in primary windings
N_s	number of turns in secondary windings
$\Delta\Theta_p$	primary winding segment arc angle
$\Delta\Theta_s$	secondary winding segment arc angle
$\Delta\Theta_{sp}$	spacing segment arc angle
$\oslash_{pa} = \Delta\Theta_p r_a$	primary inner radius arc
$\oslash_{pb} = \Delta\Theta_p r_b$	primary outer radius arc
$\oslash_{sa} = \Delta\Theta_s r_a$	secondary inner radius arc
$\oslash_{sb} = \Delta\Theta_s r_b$	secondary outer radius arc
$\oslash_{pm} = \Delta\Theta_p r_m$	middle radius winding segment arc
$\oslash_{sp} = \Delta\Theta_{sp} r_m$	middle radius winding spacing arc
h_{Mtop}	thickness of top metal layer
h_{Mbot}	thickness of bottom metal layer
h_{diel}	thickness of dielectric layer between *Mtop* and *Mbot*
h_{sub}	thickness of dielectric layer between *Mbot* and substrate

since

$$\pi = N\left(\Delta\Theta_{sp} + \Delta\Theta_{sp}\right) \tag{4.2}$$

taking into consideration that $N_p = N_s$.

4.6.2 Mutual inductance calculations

For a toroidal solenoid, the mutual inductance can be expressed as:

$$M = \frac{N_s \Phi_2}{I_1} = \frac{\mu_o A N_p N_s}{l} \tag{4.3}$$

where the parameters are as indicated by Table 4.3

Table 4.2 Definitions for electrical parameters of a toroidal solenoid transformer

Parameter	Description
I_p	current in primary windings
μ_o	magnetic permeability
Φ_s	Magnetic flux in secondary
$\epsilon = \epsilon_r \epsilon_o$	dielectric constant
C_{st}^{ps}	Side top layer winding coupling capacitances
C_{sb}^{ps}	Side bottom layer winding coupling capacitances
C_{sv}^{ps}	Side vias parasitic capacitances
C_{tb}^{ps}	Top-bottom winding capacitances
C_{tbv}^{ps}	Top-bottom vias parasitic capacitance
C_{d}^{ps}	Diagonal primary to secondary parasitic capacitance
C_{tot}^{ps}	Total primary to secondary coupling capacitances
C_{tb}^{pp}	Top-bottom winding capacitances
C_{d}^{pp}	Diagonal primary to secondary parasitic capacitance
C_{tot}^{pp}	Total primary to secondary coupling capacitances
C_{psub}^{pp}	Total primary to secondary coupling capacitances

4.6.3 Primary to secondary capacitances

The windings have several primary to secondary parasitic capacitance types. They can be classified into top-bottom, side capacitances and diagonal capacitances.

4.6.3.1 Top-Bottom parasitic capacitances

The top winding can span over more than the parts of several bottom layer windings. The top-bottom capacitance, C_{TB}, is the vertical overlap capacitance of the top layer winding to the lower layer winding and can be expressed as:

$$C_{tb}^{ps} = \int_{r_a, pri \sqcap sec}^{r_b} \frac{\epsilon \| r_x \angle (\Delta\Theta_{sp} + \Delta\Theta_p) - r_a \angle 0 \|_2 W}{h_{diel}} \tag{4.4}$$

where $pri \sqcap sec$ means that the integration is valid only when the primary winding is on top of the secondary winding. $\| \cdot \|_2$ is the 2-norm or the distance function.

4.6.3.2 Side capacitances

The side capacitance is

$$C_{st}^{ps} = \int_{r_a\Delta\Theta_{sp}}^{r_b\Delta\Theta_{sp}} \frac{\epsilon \| r_x \angle (\Delta\Theta_{sp} + \Delta\Theta_p) - r_a \angle 0 \|_2 h_{Mtop}}{s} ds \tag{4.5}$$

for the top layer, and

$$C_{sb}^{ps} = \int_{r_a\Delta\Theta_{sp}}^{r_b\Delta\Theta_{sp}} \frac{\epsilon \| r_x \angle (\Delta\Theta_{sp} + \Delta\Theta_p) - r_a \angle 0 \|_2 h_{Mbot}}{s} ds \tag{4.6}$$

for the lower layer.

4.6.3.3 Vias capacitances

The vias have sideways capacitance from primary set of vias to a secondary set of vias, at the inner radius, and can be expressed as:

$$C_{sv}^{ps} = \frac{\epsilon W \sum_{i=1}^{n} h_i}{\Delta\Theta_{sp} r_a} + \frac{\epsilon W \sum_{i=1}^{n} h_i}{\Delta\Theta_{sp} r_b} \tag{4.7}$$

where n is the number of layers where vias are introduced in the toroidal solenoid. h_i is the thickness of the metal layer where the vias are introduced. Note that this capacitance exists at the inner winding and outer radius of the toroid.

As for the number of vias that are needed, they can be determined from the current density per via.

$$n_{vias} = \frac{I_{max}}{I_{via}} \tag{4.8}$$

where I_{max} is the total current passing through the vias. I_{via} is the current per via.

4.6.3.4 Total primary to secondary capacitances

The total parasitic coupling capacitances between the primary and secondary can be written as

$$C_{tot}^{ps} = 2N \left[C_{st}^{ps} + C_{sb}^{ps} + C_{sv}^{ps} + C_{tb}^{ps} \right] \tag{4.9}$$

4.6.4 Primary to primary coupling capacitances

4.6.4.1 Top-Bottom parasitic capacitances

The top winding can span over more than the parts of several bottom layer windings. The top-bottom capacitance, C_{tb}, is the vertical overlap capacitance of the top layer winding to the lower layer winding and can be expressed as:

$$C_{tb}^{pp} = \int_{r_a, pri \sqcap sec}^{r_b} \frac{\epsilon \left\| r_b \angle \left(\Delta\Theta_{sp} + \Delta\Theta_p \right) - r_a \angle 0 \right\|_2 W}{h_{diel}} \tag{4.10}$$

where $pri \sqcap sec$ means that the integration is valid only when the primary winding is on top of the secondary winding. $\| \cdot \|_2$ is the 2-norm or the distance function.

4.6.4.2 Diagonal capacitances

The diagonal coupling capacitance of vias from primary to secondary can be written as

$$C_d^{pp} = \int_{s=0}^{s=2\oslash_{sb}+r_b\Delta\Theta_{sp}} \frac{\epsilon W \sqrt{W^2 + h_{Mtop}^2}}{\sqrt{s^2 + h_{diel}^2}} \tag{4.11}$$

4.6.4.3 Via capacitances

The capacitance from a top metal layer where the vias are located to a bottom layer can be calculated as:

$$C_{vtb}^{ps} = \frac{2\epsilon A_{via}}{\sum_{i=1}^{n} h_i} \tag{4.12}$$

This capacitance can be in series when several layers are considered for vias. This is a very small parasitic capacitance that might affect the behavior of the circuit for very high frequencies. The significance of this capacitance increases if the via matrix area is increased.

4.6.4.4 Total primary to primary capacitances

$$C_{tot}^{pp} = 2N \left[C_{tb}^{pp} + C_d^{pp} + C_{tbv}^{pp} \right] \tag{4.13}$$

4.6.5 Primary to substrate coupling capacitance

This is the sum of the capacitances to ground for the windings in the bottom layer and in the vertical connection.

$$C_{psub} = \frac{\epsilon W \| r_b \angle (\Delta\Theta_{sp} + \Delta\Theta_p) - r_a \angle 0 \|_2}{h_{sub}} + \int_{r_a \setminus 0, pri \sqcap sec}^{r_b} \frac{\epsilon \| r_b \angle (\Delta\Theta_{sp} + \Delta\Theta_p) - r_a \angle 0 \|_2 W}{h_{sub} + h_{diel}} \tag{4.14}$$

This capacitance includes the area under the vias at both ends of the winding bottom layer.

4.6.6 Optimization of toroidal transformer electrical parameters

The transformer geometrical parameters can be optimized to meet several geometrical and electrical constraints. Geometrical constraints are the area of the toroid and the thickness of the dielectric material between the top and bottom metal layer. The electrical constraints can be the Q factor, the resonance frequency of the primary, secondary. In addition, the coupling resonance frequency between primary and secondary. The self or mutual inductance and/or fitting the transformer response to an S-parameter curve, can be another set of constraints.

4.7 Characterization results in 0.18μm CMOS process

The toroidal solenoid laid out in Figure 4.3, was fabricated in 0.18μ CMOS process. A chip photomicrograph of the structure is shown in Figure 4.4, and for the whole chip in Figure 4.5. Figure 4.6 presents characterization results for the transformer using an Agilent E8364A PNA Series Network Analyzer. The results presented are preliminary results for the 2 port scattering parameters measured between the primary and the secondary. The other ports are terminated to 50Ω.

The resonance frequency, f_{res} is 6.54 GHz for this measurement from port1 to port3. The corresponding scattering parameter at resonance is $S_{13} = 0.305$. After de-embedding probe pad parasitic capacitances, $f_{res} = 8.25$ GHz with $S_{13} = 0.358$.

To reduce the substrate loss, a polysilicon shield is placed underneath the transformer. A chip micrograph of the structure is shown in Figure 4.7. This structure is chosen because it can

impede eddy current generation in the layer because of the structure nature itself. The shield bars are always perpendicular to the transformer windings to minimize the induced current in the shield. The polysilicon layer is chosen because of its higher resistivity.

Figure 4.8 presents characterization results for the transformer, with shield, using an Agilent E8364A PNA Series Network Analyzer. The results presented are for the 2 port scattering parameters measured between the primary and the secondary. The other ports are terminated to 50Ω.

The resonance frequency, f_{res} is 5.35 GHz for this measurement from port1 to port3. The corresponding scattering parameter at resonance is $S_{13} = 0.259$. After decoupling probe pad parasitic capacitances, $f_{res} = 6.69$ GHz with $S_{13} = 0.339$. S_{13} is decreased due to the shield. Further optimization is needed for a improvement in S_{13}.

Table 4.3 Characterization results of a toroidal solenoidal transformer

	No-shield	Shield
$\|S_{13}\|$	0.305	0.259
f_{res} GHz	6.54	5.35
	No-shield (Deembed)	**Shield (Deembed)**
$\|S_{13}\|$	0.358	0.339
f_{res} GHz	8.25	6.69

4.8 Challenges in toroidal solenoid transformer design

There are several challenges in the design of toroidal transformers. Most of these challenges have to be overcome for the toroidal solenoids to be usable for the high frequency circuit design.They are discussed here.

1. The thickness of the dielectric layer between the bottom layer and the top layer h_{diel} is small. It is usually less than $3 - 5\mu$m. The small h_{diel} makes the loop area small. This leads to low inductance generated in the loop. Increasing the dielectric thickness requires the use of a custom process for the toroidal fabrication.

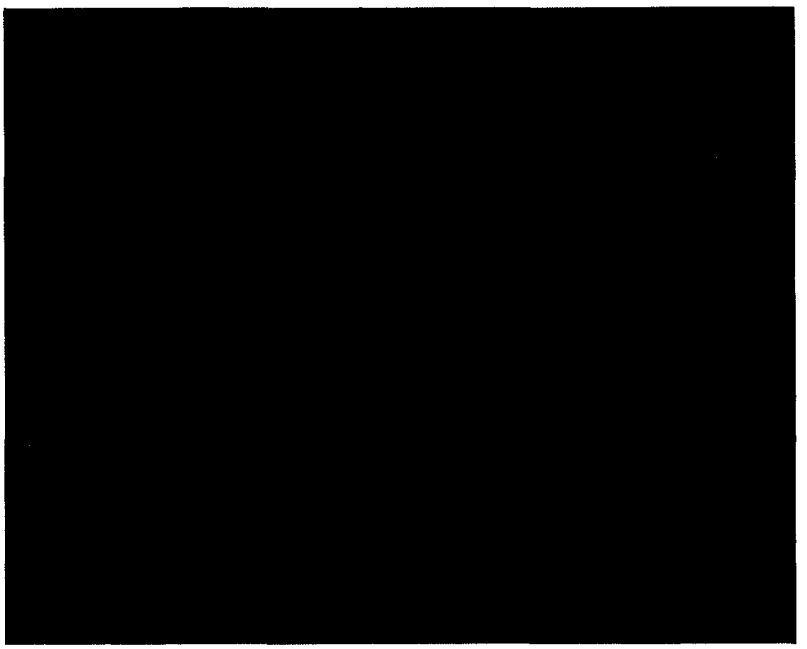

Figure 4.4 Chip micrograph of toroidal solenoid transformer *(with no shield underneath)* in 0.18μm CMOS process

2. The side parasitic capacitances between the primary and secondary is significant and can reduce the coupling resonance frequency

3. The top to bottom capacitance can be between the primary windings and the primary windings affecting the self resonance frequency of the primary or the secondary. This can also be seen at the secondary.

4. The top to bottom capacitance can be between the primary windings and the secondary windings degrading the coupling resonance frequency.

5. The long toroidal windings have a high series resistances especially at higher frequencies due to the skin effect.

These challenges can be mostly overcome by changing the structure of the transformer as shown in next section.

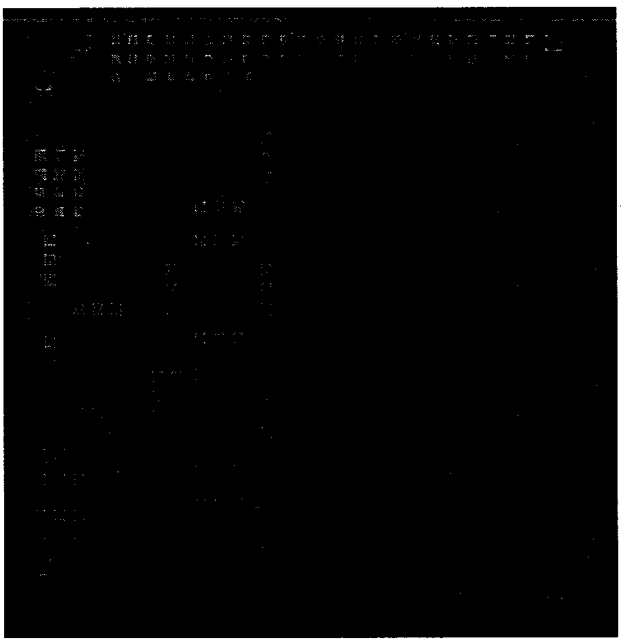

Figure 4.5 Chip micrograph of the whole chip ($3mm \times 3mm$) in 0.18μm CMOS process

4.9 Bandwidth improvement of toroidal solenoid transformers

The bandwidth of the coupling between the primary and secondary windings can be increased by decreasing the interwinding capacitance while not sacrificing the mutual inductance. The solution to this problem can be found by introducing changes in the layout of the toroidal solenoid.

The inter-level (top-bottom) winding capacitance can be reduced to a minimum by preventing any overlap between the primary and the secondary, or between any primary and primary. This can be imagined by having a spring wound into a toroid. Then, another spring of the same size and number of windings is wound into another toroidal shape. Now, the second toroid is brought to be in the center of the first toroid such that both toroids lie in the same plane, and the windings of the inner toroid get between the windings of the outer toroid. Therefore, there is no overlap between any primary and secondary toroid windings. On-chip layout is the same implementation except that structures are rectilinear, although non-rectilinear structures can

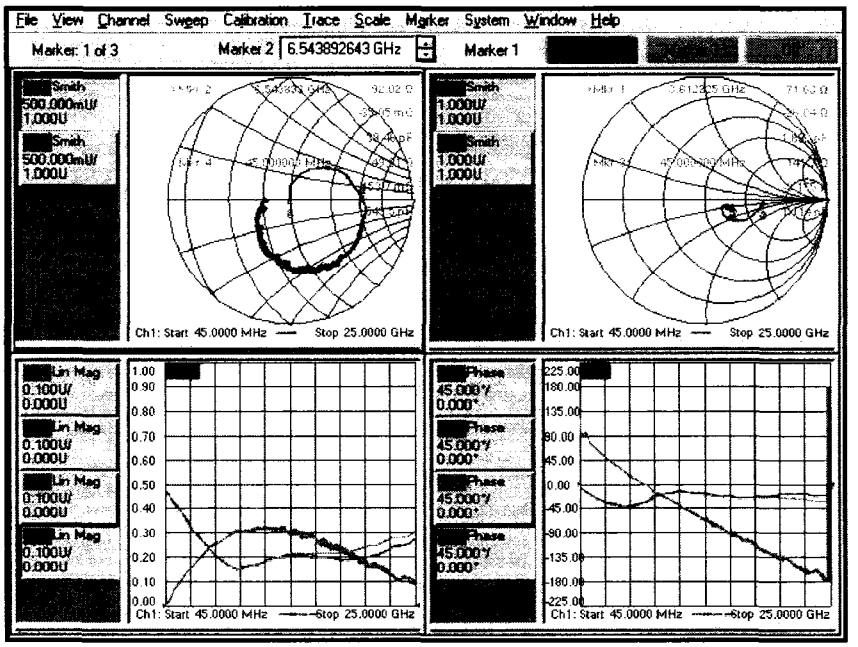

Figure 4.6 Toroidal solenoid transformer *(with no shield)* characterization results using a network analyzer

be implemented in more advanced processes. The implementation of the toroid turns out to be simple on silicon and no inter-level overlapping is maintained.

The structure described in this section is an development of the concept described in [21]. It describes a structure of a toroidal inductor where the top-bottom capacitance is minimized. The inductor structure can be modified and developed to become a transformer as described in sections 4.9.1, and 4.9.2.

4.9.1 No-overlap toroidal transformer design

An example of layout implementation is shown in Figure 4.9. This is a toroidal solenoid transformer. The connection to pads is not shown. Usually the connections can be taken from the corners of the transformer on both sides of the diagonal line. A zoom is shown in Figure 4.10. The windings of the primary are close to the windings of the secondary and at the same level. There is no overlap of windings between the primary and the secondary, the primary to primary, or secondary to secondary windings. A MATLAB script file listing, of the

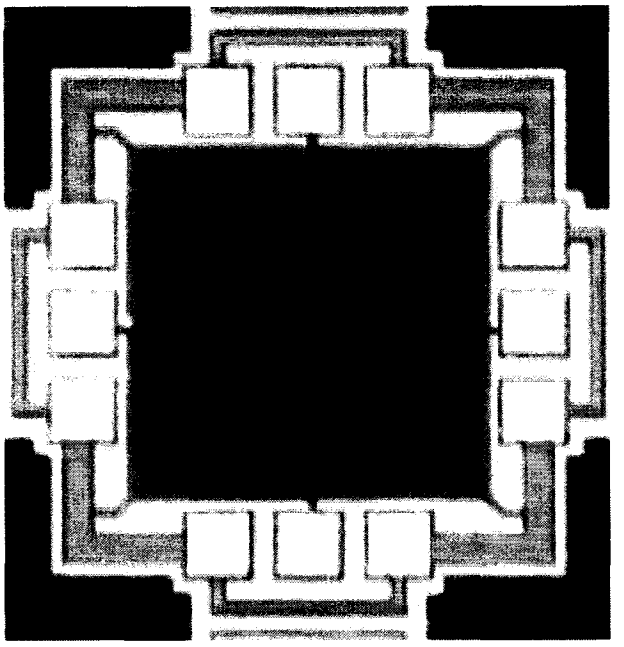

Figure 4.7 Chip micrograph of toroidal solenoid transformer *(with a polysilicon shield underneath)* in a 0.18μm CMOS

program that generates this structure in ASITIC, is in Appendix B.3.

4.9.1.1 Inductance and capacitance calculations

The mutual inductance calculations are subject to Eqn 4.3. As for the parasitic capacitances, they are simpler to calculate than in section 4.6. The self parasitic capacitance is only to the substrate. The coupling capacitance between primary and secondary is only the side to side capacitance at the bottom and the top layers. Since the capacitance is decreased dramatically, the resonance frequency f_{res} is improved greatly because of this architecture.

4.9.2 Minimal capacitance toroidal transformer design

The contribution of the parasitic side capacitances mentioned in the previous section can be minimized to a fringe factor by introducing layout changes to the structure in Figure 4.11, and Figure 4.12. This can be done if the winding segment of the primary is laid out in the lower (upper) layer, the winding segment of the secondary that is adjacent to the primary is

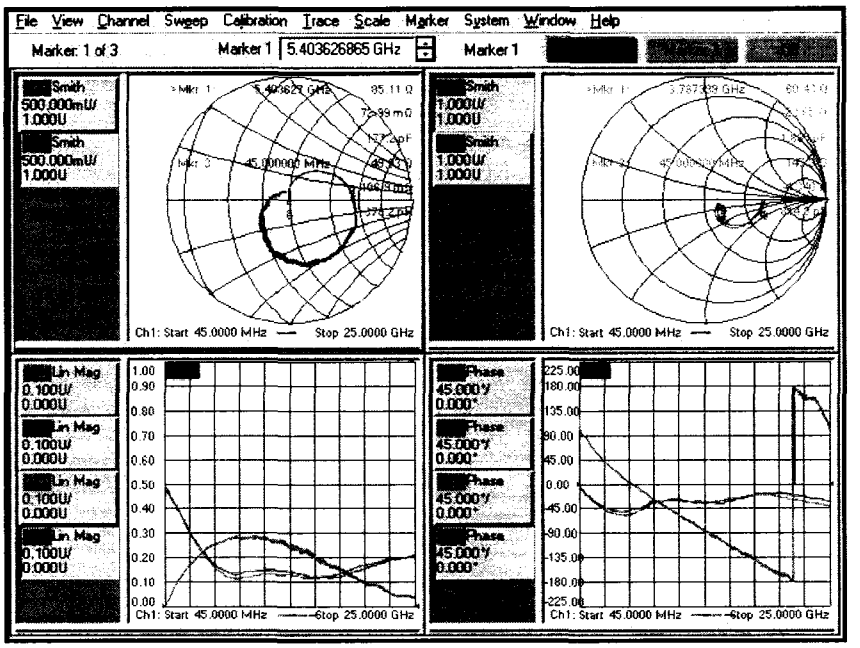

Figure 4.8 Toroidal solenoid transformer *(with shield)* characterization results using network analyzer

laid out in the upper (lower) layer. In this way, the only contribution of this factor is close to the via when the layers change, introducing very small contribution of capacitance to this factor. A top view of an example toroidal transformer with this feature is shown in Figure 4.11. Figure 4.12 shows the primary windings separated from the secondary windings with no side capacitances except the minimal capacitance at the via corners. A MATLAB script file listing, of the program that generates this structure in ASITIC, is in Appendix B.2.

If the self winding capacitance to substrate is to be minimized, the first metal layer needs to be built on a thick oxide layer of around 5μm. Another solution is to etch the substrate underneath the toroid. Air can replace the etched substrate and air replaces the substrate. In this way, the self capacitance to ground can be minimized too.

If the toroidal solenoid is to be implemented on chip, with a custom process, it will provide a high k coupling and high resonance frequencies, and the magnetic flux will be contained to the toroidal structure, and not injected to the substrate as in the case of interleaved and concentric transformers.

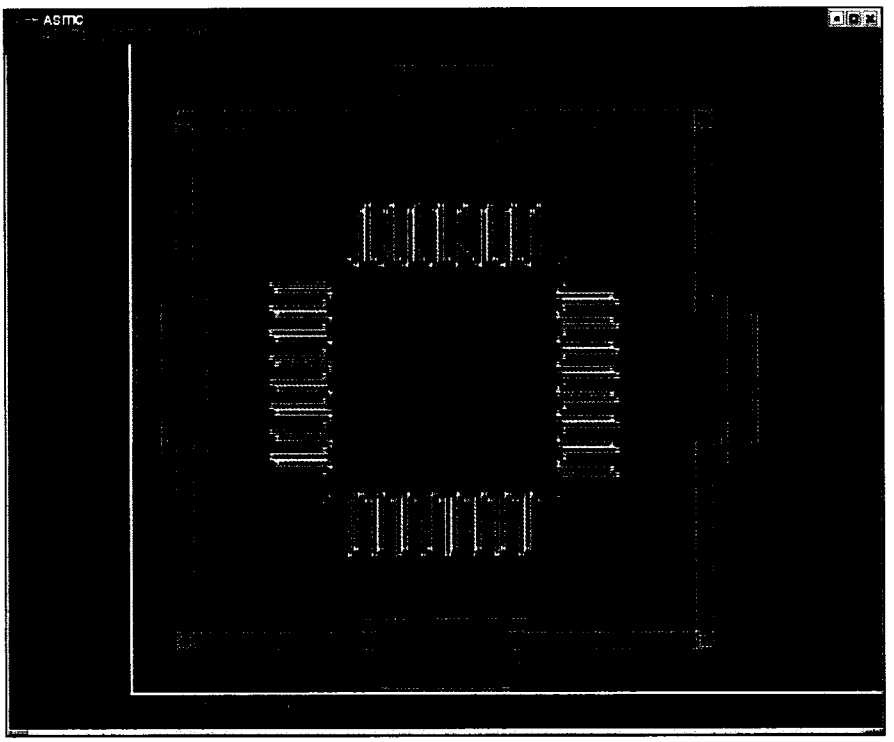

Figure 4.9 Non-overlap toroidal solenoid in ASITIC *(connection to pads not shown)*

4.10 Implementation in custom ISU 2u process

A chip containing several toroidal solenoid structures was designed in Custom ISU 2u process. The great advantage of this process is that it can be completely customized by the designer. Twelve Toroidal solenoid Transformers were designed and laid out. Since the whole wafer can be utilized for the layout for a fixed charge, the total area was about 10mm X 12mm.

Four 2u chromium masks were generated. The first mask was for the substrate contacts. The first metal layer occupied the second mask, while the Inter-metal vias were generated by the third mask. The final mask was for the upper metal layer.

The design of the process was to grow a 5u thick oxide layer on the substrate first. Then an aluminum metal-one layer is grown with thickness of around 3u in order to reduce the ohmic

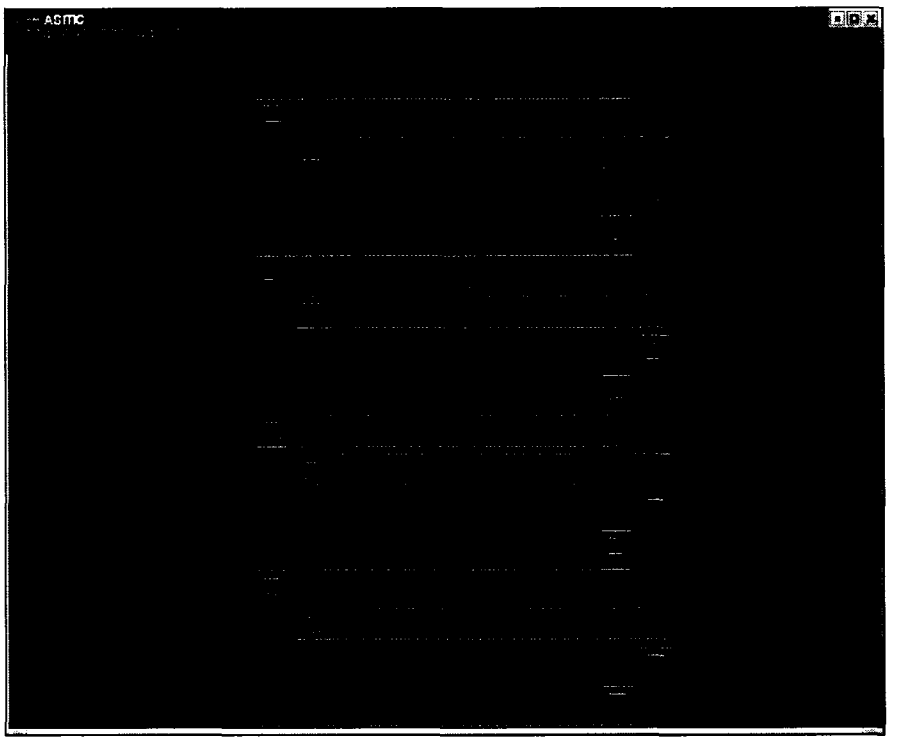

Figure 4.10 Non-overlap toroidal solenoid in ASITIC *(zoom)*

loss. A thick oxide layer is grown between the lower metal layer and the upper metal layer. This thickness is around 15um. This can be achieved by using the same via mask three times. Finally, the top metal layer is grown using 3μm aluminum.

Up to the writing of this dissertation, the Plasma Enhanced Chemical Vapor Deposition (PECVD), had a pressure leak. The formation of the silicon wafer was halted till the equipment is restored. A layout of the negative layers of the test chip is shown in Figure 4.13.

4.11 Contribution summary

In this chapter, analysis of monolithic integrated transformers is presented. Several toroidal transformers were fabricated in a 0.18μ CMOS process. Characterization results show a resonance frequency above 5GHz for a toroidal transformers with an $|S_{13}| > 0.3$.

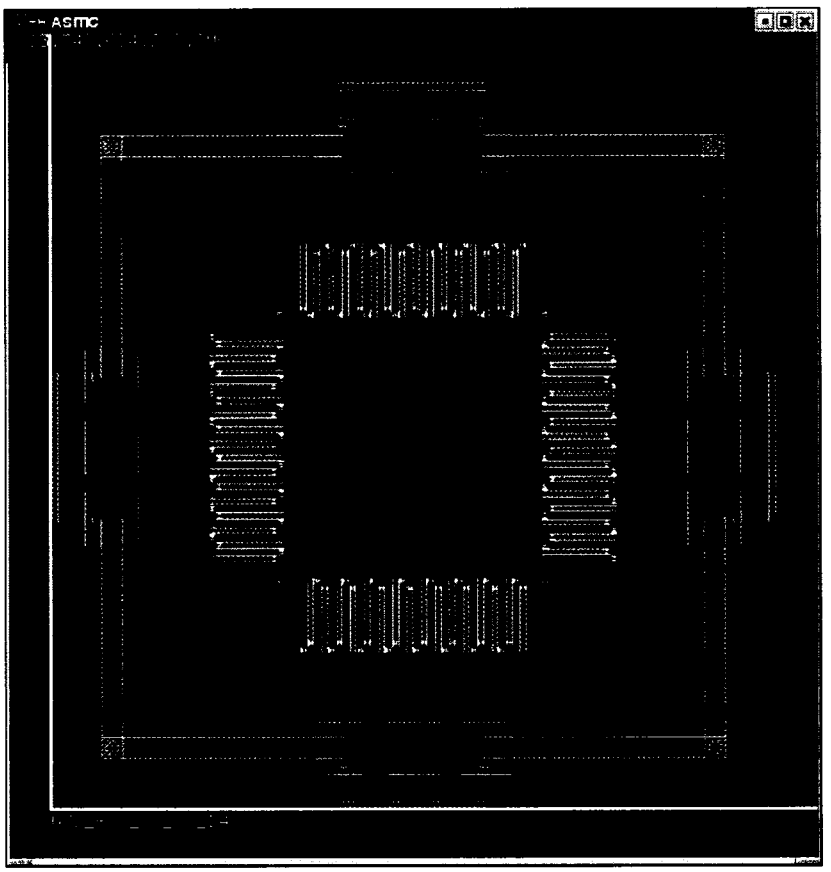

Figure 4.11 Minimal capacitance toroidal solenoid in ASITIC *(connection to pads not shown)*

Other structures are developed where the self or coupling parasitic capacitances are minimized to maximize the resonance frequency of the transformer and improve its performance parameters. This structure depends on the concept of eliminating the overlap of top-bottom metal layers, and maximizing the horizontal distance between the windings in the same layer to minimize the parasitic capacitances. The structures are intended to be fabricated in the custom ISU 2μ process.

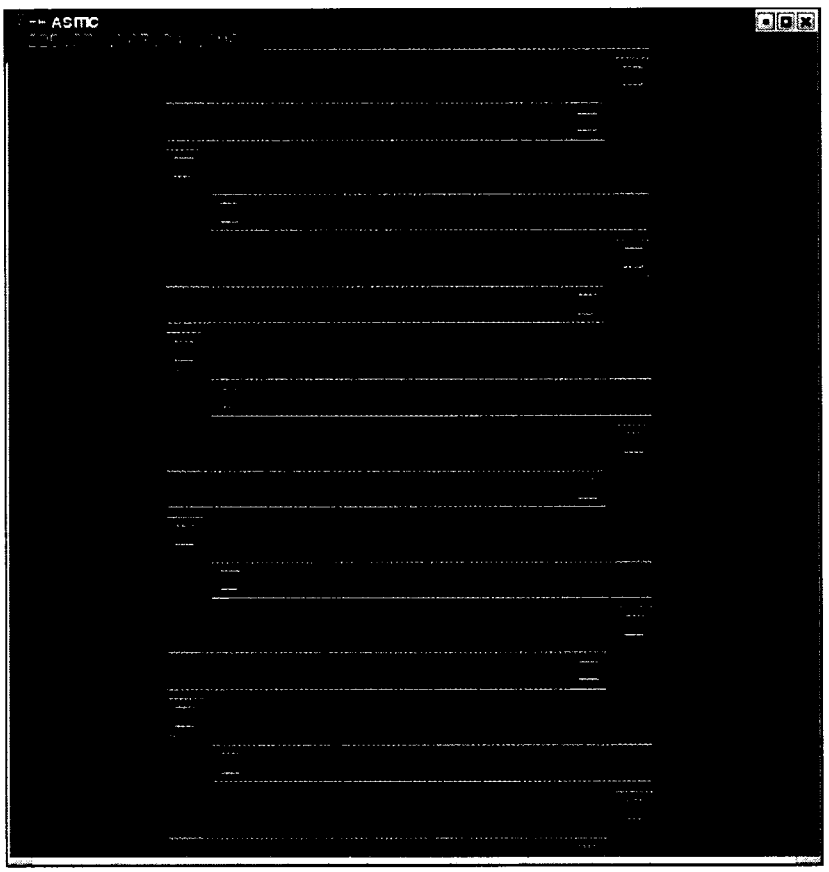

Figure 4.12 Minimal capacitance toroidal solenoid in ASITIC *(zoom)*

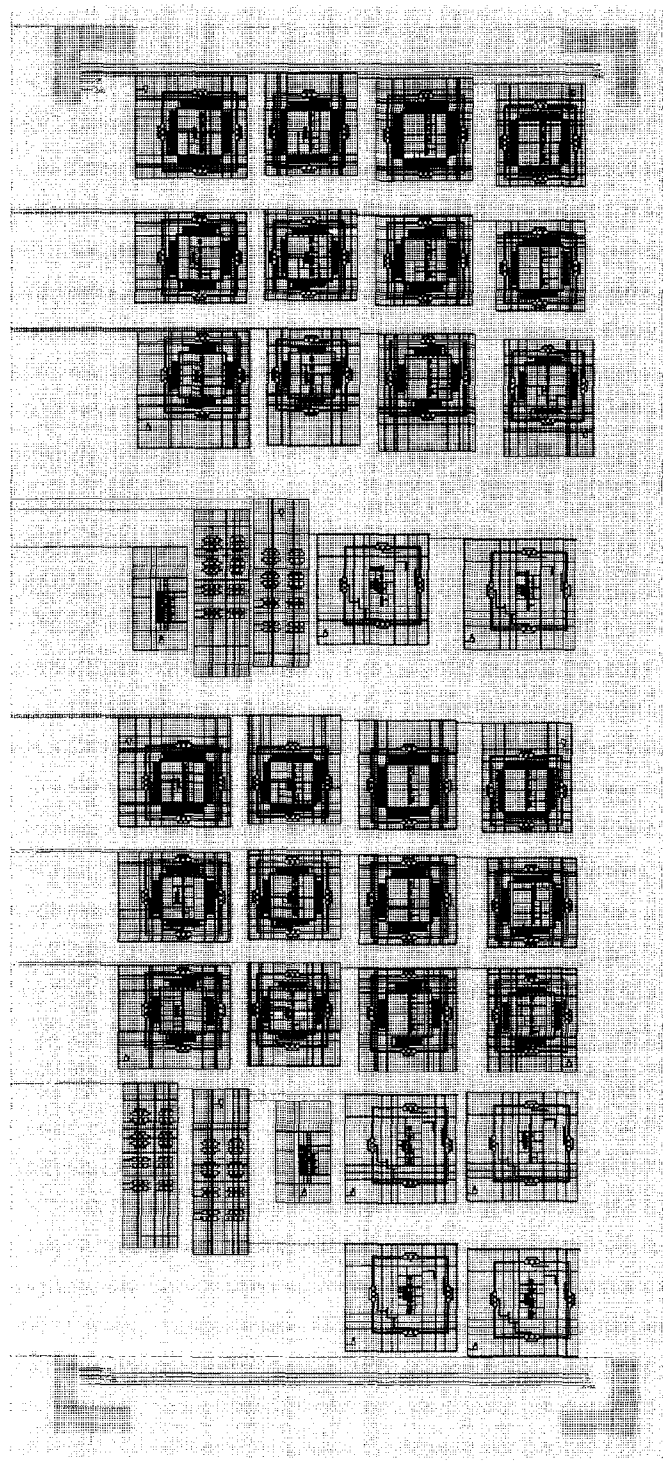

Figure 4.13 Negative layout of test chip in ISU 2u process*(zoom)*

CHAPTER 5. Microstrip line modelling

5.1 Introduction

In this chapter, the design of edge coupled microstrip lines (MSL) is discussed. They are placed between the chips on the printed circuit board. The choice of the MSLs depends on several factors and the priority of these factors. One of these factors is the speed of the signal that needs to be transmitted along the line. Another factor is the level of electromagnetic interference that the interconnection circuit has to comply to. In this chapter, the choice of laminate material for the PCB is discussed. Several laminate material features are analyzed. Simulations of the power transmission and loss in the signal, while being transmitted through the MSL are presented.

5.2 Laminate materials analysis

5.2.1 FR4 laminate material

The most common choice of laminate material for low frequency use is FR4 material because of its cost, and because it doesn't need a special process to manufacture and to print the metal layers on it. However, there are several problems with this material when we try to implement it for high-speed digital data transmission. Below is a brief discussion of them.

The problem with this material is its dissipation factor, $\tan(\delta)$, at 1 MHz. This is an order of magnitude higher than most other materials. Knowing that the attenuation factor, $\alpha_D = \pi f \tan(\delta)\sqrt{LC}$, is a direct function of both the dissipation factor and frequency, this leads to a very poor performance at Giga-Hertz frequency range. This can be demonstrated in different frequency components of the signal being attenuated at different rates depending

on the frequency. This creates distortion in the signal shape.

The other disadvantage of FR4 material is its high dielectric constant, $\epsilon_r \simeq 5.4$, which means that signal is transmitted at a lower propagation velocity than for other materials with lower dielectric constant. The other problem associated with FR4 materials is the variation of its dielectric constant with frequency and its reproducibility. Since the propagation velocity, v, depends on ϵ_r, $v = c/\sqrt{\epsilon_r}$, this would result in different frequency components of the signal arriving at different times at the receiver. This leads to a phase distortion in the received signal.

5.2.2 Microwave laminate materials

Due to all of the above problems associated with the use of FR4, other materials were also considered such as GML1000 [17], and Rogers 4003 [18]. These materials are primarily used for microwave applications. As shown in Table 5.1, the GML1000 material is very comparable is performance to Rogers4003 material.

Table 5.1 Comparison of different laminate materials

	$\tan\delta$		ϵ_r		Cost (normalized) (18" × 24")
FR4	< 0.03	@ 1 MHz	< 5.4	@ 1 MHz	1
GML1000	0.003	@10 GHz	3.05	@ 10 GHz	1.33
Rogers 4003	0.0027	@10 GHz	3.38	@ 10 GHz	10.03

The dissipation factor is almost the same for both materials. For GML1000, the dielectric constant is smaller than the one for Rogers4003. In the last column, the cost of one laminate PCB is almost an order of magnitude smaller for GML1000 than for Rogers4003. Because of the difference in cost, GML1000 material is used in simulation and analysis.

5.2.3 GML1000 and FR4 laminate material comparison

In this section, a comparison analysis between FR4 and GML1000 materials is performed. From Table 5.1, it can be seen that GML1000 material enjoys having much smaller $\tan(\delta)$ than FR4. This results in much less attenuation of the transmitted signal at higher frequency. If a

data transmission speed up to 10 Gbit/s RZ code, or 20 Gbit/s NRZ code is considered, then frequency contents, up to 10 GHz, are required for analysis.

The objective of the analysis is to compare the s-parameters of both laminate types. This will give a good indication of how the frequency components of the transmitted signal are attenuated at the received end.

An HSPICE FS simulation file was written in order to generate the RLGC matrices of the TL placed on FR4 laminate PCB. A similar simulation file is found in A.1 for a transmission line (TL) placed on GML laminate PCB. Afterwards, an HSPICE circuit simulation file is written to generate the S-parameters for the TL. A similar file is listed in A.2. The output of the simulation is a table of S-parameters graphed in Figure 5.1.

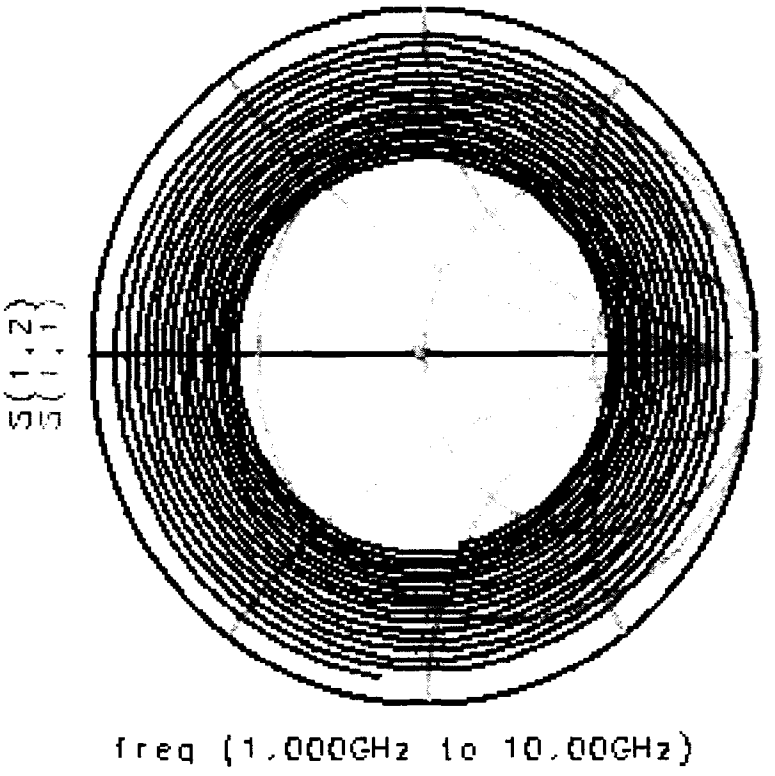

Figure 5.1 S_{12} (dB) in blue and S_{11}(dB) center red dot in FR4

This graph is for the S-parameters of the FR4 material. S_{11}(dB) is placed in the center of the smith chart where the TL is terminated with an impedance almost equal to the charac-

teristic impedance of the transmission line. Since S_{11}(dB) is the TL reflection coefficient, then this ensures that no signal power is reflected back from the transmitter. Note that $S_{11} = S_{22}$ in this case since the TL is terminated equally at both ends.

As for S_{12}, it represents the transmission coefficient of the signal. At low frequencies, 100 MHz, almost all of the signal is transmitted along the TL. Therefore S_{12} is almost 1. As the frequency increases, the phase distortion of the signal, due to the transmission, appears visible in the spiral path that S_{12} takes. S_{12} decreases in magnitude because of the higher attenuation the signal experiences as the frequency gets into the GHz range. If the TL is very long, then S_{12} reaches the center point eventually. Figure 5.2 shows S_{11} and S_{12} plot on a smith chart as a function of frequency from 0.1 GHz to 10 GHz. The material investigated is GML1000. S_{11} can be seen as a small dot in the

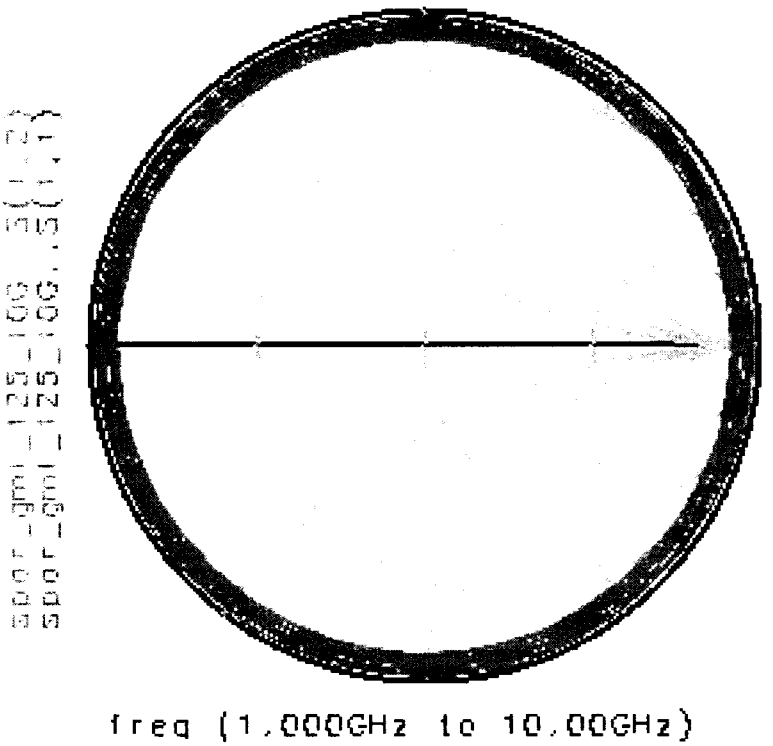

Figure 5.2 S_{12}(dB) in blue and S_{11}(dB) center red dot in GML

center of the smith chart. For any frequency, it can be observed that the S_{12} magnitude is larger for a TL on a GML1000 material as in Figure 5.2, than for a TL on an FR4 material as

in Figure 5.1. This clearly demonstrates the lower loss feature of GML1000 materials.

Figure 5.3, illustrates the magnitude of attenuation of the signal, as a function of frequency, for TL's on FR4 PCBs, and GML1000 PCBs. Note that at 10 GHz the attenuation in the FR4 case is more than -5dB for 10cm. On the other hand, the GML1000 case achieves an attenuation of less than -0.8dB.

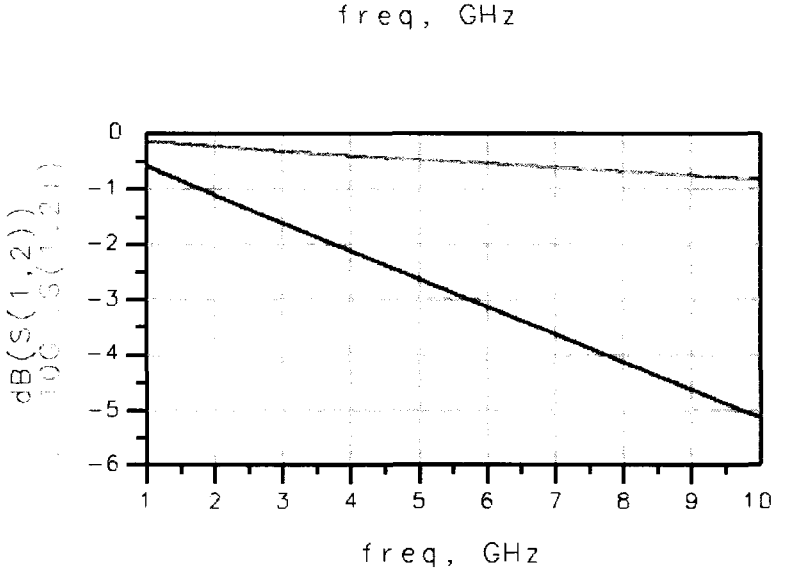

Figure 5.3 S_{12}(dB) in FR4, lower blue, and GML1000, upper red

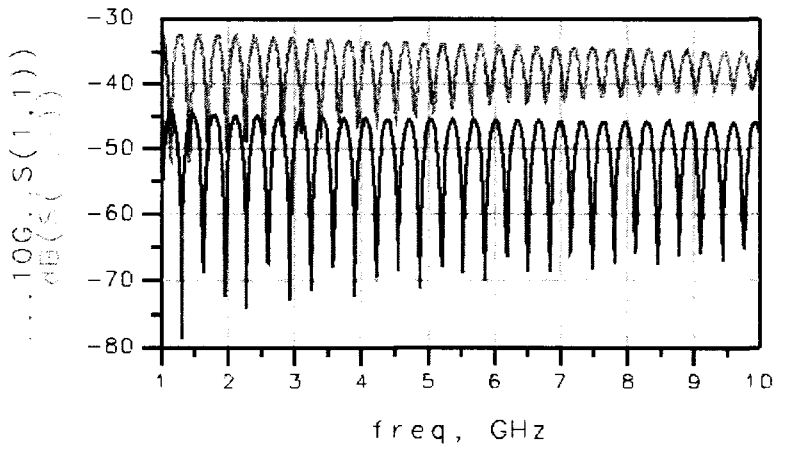

Figure 5.4 S_{11}(dB) in FR4, upper red, and GML1000, lower blue

Figure 5.4 shows S_{11}(dB) for both FR4 and GML cases. The significance of this illustration

is to show that S_{11} in both cases is very small, under -40 dB. This represents good matching. The peaks and bottoms present that the matching is not completely perfect and depends on frequency. This matching is needed to have a proper test setup.

5.3 Contribution summary

This chapter provides a brief comparison study of GML1000 and FR4 materials for PCB circuits. In this chapter it is proposed that GML1000 material might be preferable over FR4 material for high speed circuits. This is due to the higher performance characteristics of the GML1000 material such as a stable ϵ_r over a large frequency range, low loss factor, cost and compatibility with standard manufacturing process.

CHAPTER 6. Bonding wire modelling toolbox in HSPICE and MATLAB

6.1 Introduction

This chapter discusses modelling the bonding wire (BW), which is a metal wire that is usually made of gold and connects the chip pad to the PCB pad, or to the lead pins of the package. At low frequencies, the parasitic resistance and inductance of the BW have minimal negative effect on the quality of the signal that passes through the BW and into or out of the chip. The electrical model for the BW is needed to be included in the simulation of a high frequency serial link especially in the GHz frequency range.

The BW models that are currently used in circuit design consist of lumped elements of inductors and capacitors, and resistors. While these models can accurately describe the electrical behavior of BW at relatively low frequencies, these models are not accurate enough to describe the BW at frequencies in the GHz range. One of the reasons is the skin effect of the resistance of the bondwire. The resistance becomes a function of frequency. In addition the inductance itself changes with frequency. Therefore a distributed model is developed to capture the different parasitic effects.

Several approaches already exist in BW modelling. One approach is to perform a full 3D electromagnetic modelling using FastHenry[32] software as in [56]. In [51], FastHenry was used to model the bondwire. In order to capture the curvature of the bondwire, 3D pictures are taken for the actual bondwire, and a special software analyzes the pictures to create a mathematical model for the curvature. A different approach models the BW as a straight line structure as in [33] where the simulation is performed by a commercially available 3D electromagnetic software programs.

6.2 Objective of research

The objective of the research in this chapter is to provide a fairly accurate electrical model for the BW. This model is in the form of a subcircuit model that can be used in HSPICE[30] simulations for a high speed serial link. The model does not use a 3D electromagnetic simulator. Instead, it uses an HSPICE 2D Field solver. It simulates the BW at many sections to emulate a third dimension along the path of the BW. The BW assumes a Chip on Board (COB) assembly. This is the choice of the packaging at high frequencies to eliminate the self parasitic capacitances and inductances, and the mutual capacitances and inductances of the lead pins.

6.3 General description of BW modelling and design toolbox

The bonding wire transmission line model is generated in HSPICE using the Field Solver (FS) capability. Matlab is used as an interface that generates the HSPICE simulation input files, and runs HSPICE within Matlab to generate the output files. Since the data is sent differentially, a pair of BWs is analyzed instead of a single BW, unless otherwise mentioned, throughout this chapter.

The BW model makes use of the W-model that is offered in HSPICE 2001.2 edition. The W-element is a subcircuit that is able to model the frequency dependence of the resistance and conductance of the transmission line. The W-element is an improved step over the U-element where the resistance of the transmission line is not a function of frequency and the model. The U-element can only accurately model the transmission line at one frequency that should be provided by the designer. The U-element does represent the transmission line accurately if the signal power is spread over more than one frequency in the frequency spectrum.

The BW toolbox allows for the electrical analysis of the BW characteristics like Z_o, Z_{odd}, and Z_{even}. It simultaneously produces a geometric 3D model to aid in the analysis. The BW toolbox can be used in high speed design. Many variables whether geometrical or electrical can be tuned and optimized to achieve the electric and geometric goals design.

6.4 The method of modelling

There are two types of modelling involved. The first is a 3D geometrical model of the BW itself generated in Matlab and described in Section 6.5. The second is an electrical model, described in Section 6.6, of the BW generated in Matlab and HSPICE that can be plugged in as a sub-circuit in simulations.

6.5 Geometrical model

In the geometrical model, a chip on board model is developed. The substrate, and metal layers of a two layer PCB are modelled. A chip dielectric material and top metal layer are modelled on top of the PCB. Finally, a 3D geometric bondwire is modelled and represents the connection between PCB traces and on chip pads. A 3D geometric model of the structure is developed as shown in Figure 6.1. Table 6.1 lists the input parameters to the geometric model. Note that these parameters are also used for the electrical model as well.

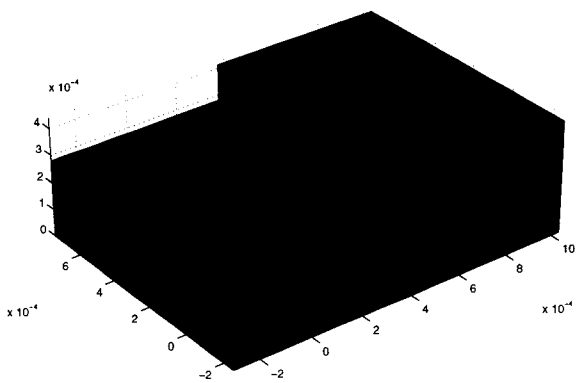

Figure 6.1 3D View of bondwire model with chip and PCB shown

6.5.1 Substrate model

There are two types of substrates: The PCB substrate and the chip substrate. The PCB substrate is built using HSPICE FS. The material used for simulation is a GML 1000 laminate

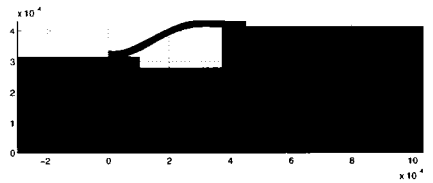

Figure 6.2 Side view of bondwire model with chip and PCB shown

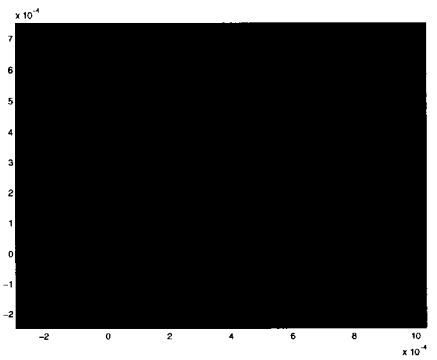

Figure 6.3 Top view of bondwire model with chip and PCB shown

material as in Figure 6.1, 6.2, and 6.3. It's a two metal layer material where the dielectric material (green) lies between the upper and lower metal layers. The bottom layer is ground (blue) while the upper layer consists of signal traces layer (purple). The PCB pads are modelled in the top metal layer of a PCB.

Figure 6.2 presents a side view of BW. It is modelled in the following way. First, a thin layer of insulation glue separates the PCB from the chip. Then the substrate of the chip is modelled on top of that. The chip dielectric material is modelled up to the top metal layer (collectively shown as Cyan). Afterwards, the PCB pads are modelled in the chip top metal layer.

Table 6.1 Input geometrical parameters to BW toolbox

Parameter	Typical value	Description
		Printed Circuit Board
tg	35×10^{-5}	Thickness of GND plane of PCB
hp	1.5×10^{-3}	Thickness of dielectric layer of PCB
tp	35×10^{-5}	Thickness of bondpad of PCB
wp	250×10^{-6}	Width of bondpad of PCB
spacep	200×10^{-6}	Inner edge to edge distance for PCB pads
pp	125×10^{-6}	Extension of PCB bondpad under bondwire
msl_len	.5	length of PCB microstrip line in m
		Chip
wc	50×10^{-6}	Width of bondpad of chip
space	50×10^{-6}	Inner edge to edge distance for chip pads
pc	25×10^{-6}	Extension of chip bondpad under bondwire
tc	9×10^{-7}	Thickness of bondpad of chip
hc	7.4×10^{-4}	Thickness of dielectric layer of chip
		Bondwire
nop	100	number of BW segments generated
rad	25×10^{-6}	Radius of bondwire

6.5.2 Bonding wire model

A 3D geometric model of the wire is developed. It consists of a set of horizontal cylindrical cross-sections along the path of the BW, which spans from the PCB pad to the chip pad. The solid cylinder radius is fixed for all cross-sections, and equals to the radius of the BW. There is a room of improvement here where the cross section of the BW can be improved to be parabolic, where the BW angle is steeper, that mimics more the actual cross section of the BW. The present case assumes that the elevation angle of the bondwire is not steep along the path from PCB to chip.

Consider a top view of the BW plane as in Figure 6.3. In addition, assume that there is a centerline that can be drawn from the center point between the chip pads and the PCB pads. Then the axis of the cylinder is always parallel to that centerline.

The number of cross-sections needed along the path and the length of the cylinder are

Table 6.2 Input electrical parameters to BW toolbox

Parameter	Typical value	Description
		Printed Circuit Board
`condc`	57.2×10^6	Conductivity of chip metal
`erc`	4.1	Dielectric constant of chip dielectric material
`ltc`	2.7×10^{-3}	Loss tangent of chip dielectric
		Chip
`condp`	57.2×10^6	Conductivity of PCB metal
`erp`	3.05	Dielectric constant of PCB dielectric material
`ltp`	2.7×10^{-3}	Loss tangent of PCB dielectric
		Bondwire
`condbw`	57.2×10^6	Conductivity of bondwire

determined by the frequency content of the signal that is transmitted along the BW. Consider a metal interconnect through which a high frequency clock signal is passing. The signal wavelength can be calculated as

$$\lambda = \frac{c_0}{\sqrt{\epsilon_r}} \tag{6.1}$$

where c_0 is the speed of light, ϵ_r is the effective dielectric constant of material. f is the frequency of operation.

For the metal interconnect, with length l, to be considered as a transmission line, $l \geq k\lambda$. k is constant around 0.1.

Note that for a 5GHz clock in a 10Gbit/s serial link over a GML1000 material, $\epsilon_{r,eff} < 3.05$. Then $\lambda > 3.4 \times 10^{-2} m$. The length of the bondwire ranges from 450μm, in the case of COB assembly, to $1 - 4$ mm in the case of a larger package with leads.

The BW segments lengths are intentionally made small in the toolbox so that the curvature of the BW is considered in the analysis. For the geometrical model, the BW segments are on the order of 100 segments per $0.5mm$. That's 5μ m per segment.

The final electrical model can be just few segments that capture the cases of curvature such as:

- BW on metal on PCB

- BW on PCB dielectric
- BW on metal on chip

and can be built into the subcircuit model.

As for the curvature of the BW, it can be modelled using a few coordinate points. The coordinate pairs are the distance from the PCB pad center along the centerline between the BWs, and the vertical distance from the PCB metal layer.

6.6 Electrical model

The electrical model of the BW is generated in HSPICE using Matlab as an interface. The geometrical parameters, listed in Table 6.1, and the electrical parameters, listed in 6.2 are needed for simulation. HSPICE Field solver tool is utilized. Since an HSPICE simulation file is needed for each section of the BW, therefore the HSPICE input files are generated automatically through Matlab. Figure 6.13 describes the data flow and generates files in Matlab and HSPICE. The simulation starts with the differential microstrip line as in Figure 6.4. There are three different Matlab files, where each is used for each BW stage. The files are:

1. `bw_o_pcbpad.m` BW over PCB pads.
2. `bw_o_diel.m` BW over dielectric material of PCB.
3. `bw_o_chippad.m` BW over chip pads.

These files are called by a Matlab function called `gen2m.m`. The output of these files is `bw_seg.sp` used as input to HSPICE FS. After the field solver is finished with simulating `bw_seg.sp`, it is deleted and regenerated again for the next BW segment. In this way, minimum usage of disk space is achieved. The output of the field solver for each segment, `bw_seg.sp`, is the RLGC set of matrices for the BW segment. The sets of RLGC matrices for each BW segment are collected into `seg.rlgc` file. This file will be recalled in the future to retrieve the RLGC matrices for each segment in the BW during HSPICE simulations.

Figure 6.4 Cross section of PCB with PCB interconnect

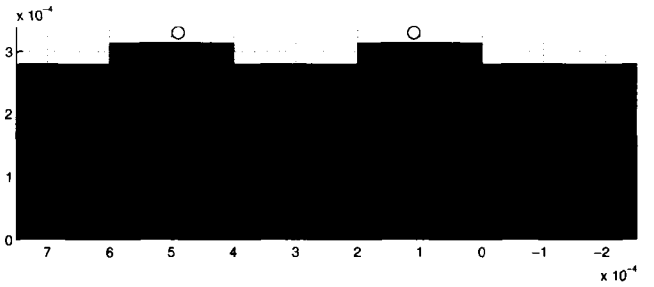

Figure 6.5 Cross section of BW on PCB with PCB interconnect

6.6.1 Bonding wire cross-sections

The vertical cross-sections of the layout along the BW path are described in more detail.

In the 3D geometrical model, if vertical cross-sectional views of the BW were considered, as in Figure 6.3, it can be seen that the number of metal layers and dielectric vary along the BW path. In the first stage, a model of the microstrip line is generated as in Figure 6.4 very

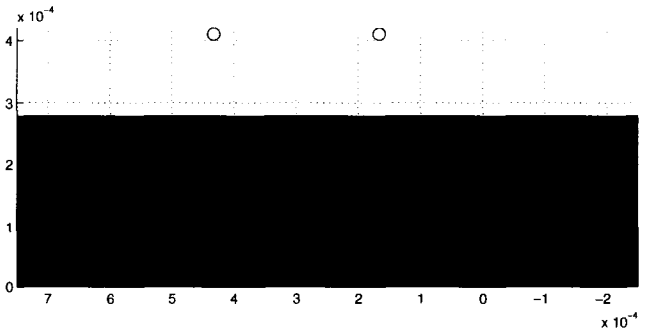

Figure 6.6 Cross section of BW on PCB without PCB interconnect

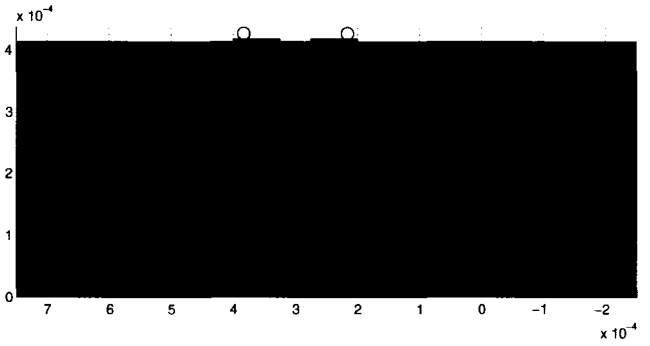

Figure 6.7 Cross section of BW on chip with PCB traces

close to the PCB pads, the BW is on top of the PCB pads and at the same time on top of the PCB top layer as in Figure 6.5. This situation occurs because the BW is bonded to the center of the PCB pad, and not to its edge. Thus leaving some extra part of PCB pads underneath the bondwire as in Figure 6.5.

The second stage is when the BW is on top the PCB, and over the dielectric material. This stage usually covers most of the BW path. The third stage is when the BW is above the chip pad before it reaches the center of the pad as in Figure 6.7. This is a small section of the path. Note in this case that we have a chip pad and then the chip is on top of the PCB.

6.6.2 Bondwire circuit model

Matlab also generates the file `bw_sub.lib`. This file is the BW sub-circuit model that can be used with other circuit elements like transistors, capacitors, etc in regular HSPICE simulations such as transient and AC analysis. Please note the following on the `bw_sub.lib`. The W-element in this sub-circuit has two variations taking into consideration if the BW is above a pad or above a dielectric layer.

1. If the BW is above dielectric only then the number of ports is only four. Two for the input ports and two for the output ports of the BW pair.

2. If the BW is above a pad then the W-element has four inputs ports: two for the BW pair, and two for the pads that are underneath it. In addition it has four output ports:

two for the BW pair, and two for the pads that are underneath it.

The four-port output of the BW W-element is connected to the 2-port input of the BW W-element in the following way as shown in C.12. The two output ports of the pads, in the 4 output ports of the BW are connected to a very large resistance $\sim 100M\Omega$ and not connected to the next segment. The other two ports of the four output ports of the BW are connected to the two input ports of the two-port BW. Since the BW lands on the center of the pad then, electrically, the BW segment and the pad that lies directly underneath it assumed to have the same potential. Therefore, a very small resistance is added between the BW segment and the pad segment underneath it. Consequently, this arrangement effectively shorts them together.

In summary, `bw_sub.lib` subcircuit is a 2 port i/p and 2port o/p network. The 8 port elements above are internally terminated to high resistance to simulate an open circuit in the case of pad extension under BW, or as a short when the BW touches the PCB or chip pads.

6.7 Bonding wire analysis

6.7.1 Introduction

In this section, an analysis of the BW electrical parameters such as the odd mode, and even mode characteristic impedances, is performed. The Matlab interface developed allows for a lot of variations in the BW position, shape, thickness, spacing between pads, and many other options as in 6.1, and 6.2. Therefore, a lot of analysis can be performed on the BW model to produce an electrical model with an optimal performance depending on the application.

6.7.2 Bonding wire optimization problem

Generally speaking, the BW performance problem can be mathematically formulated as a nonlinear constrained optimization problem. The optimization function can be to minimize the error in the characteristic impedance relative to a reference impedance. The objective function can be formulated as:

$$\min_{variable} \|Z_{o,desired} - Z_{o,simulated}\| \tag{6.2}$$

such that

$$lowerbound \leq variable \leq upperbound \tag{6.3}$$

$$\tag{6.4}$$

where *variable* can be any or all of the parameters in Table 6.1, electrical variables, as in Table 6.2 characteristic impedance depending on the driver output impedance and the PCB traces. The optimization problem can be nonlinear. Several nonlinear optimization algorithms, summarized in [4], can be utilized in reaching a local minimum for this error function.

6.7.3 Bonding wire characteristic impedance

The general characteristic impedance of a single BW can be written as

$$Z_o = \sqrt{\frac{R + jwL}{G + jwC}} \tag{6.5}$$

where R is the resistance of the conductor in Ω/m. L is the inductance of the conductor in H/m. G is the conductance of the conductor in mho/m. C is the capacitance of the conductor in F/m. Since the information is sent differentially over a pair of BW, then the parameters that we need to investigate are the even mode and odd mode characteristic impedances.

6.7.4 Odd mode and even mode characteristic impedances

The case of odd mode signal propagation happens when a differential signal is sent on a pair of transmission lines. In the present case the transmission line is in the form of BW pair. Since the currents passing through the BW pair are equal but are 180 out of phase then the effective inductance seen by each BW will be the self-inductance minus the mutual inductance between the BWs [2]. In mathematical terms, for two conductors:

$$Z_{odd} = \sqrt{\frac{L_{11} - L_{12}}{C_{11} + C_{12}}} \tag{6.6}$$

where $C_{11} = C_{1g} + C_{12}$. C_{1g} is the self capacitance to ground.

Since the voltage on one BW is equal in magnitude but 180 out of phase to the other voltage, the effective capacitance between the BWs is the BW self-capacitance to ground in addition to twice the mutual capacitance seen between the BWs. As a result, the effective capacitance increases [2].

$$Z_{even} = \sqrt{\frac{L_{11} + L_{12}}{C_{11} - C_{12}}} \tag{6.7}$$

where $C_{11} = C_{1g} + C_{12}$, L_{12} is the mutual inductance between BWs, and k is the coupling coefficient.

6.8 Design example for Chip on Board

Figure 6.8 shows the self characteristic impedance of one of the BWs in a BW pair. Two design variables were varied. The first one is the BW radius while the second one is the spacing between the chip bonding pads.

In Figure 6.8, the BW height is plotted in a thick gold color from the PCB pads to the chip pads. In general, there are several trends along the BW path. Z_o begins at the point where the BW intersects with the PCB pad center. $Z_o = 120\Omega$. Z_o increases gradually till the distance $x = 1 \times 10^{-4}$. This is due to the gradual lifting of the BW from the PCB metal pad. For $10^{-4} < x < 4.2 \times 10^{-}4$, the BW pair is just above PCB dielectric. Z_o increases sharply just after $x > 10^{-4}$. This happens when the BW passes the PCB metal under it. When $x > 4.2 \times 10^{-4}$, the BW passes over the chip pads, and Z_o drops abruptly and reaches $205 - 230\Omega$ depending on the design variables.

For a constant BW radius, increasing the chip pads spacing from 50μm to 200μm increases Z_o close to the chip edge. For example, when keeping BW radius constant at 10μm, changing the spacing from 50μm, blue curve, to 200μm, magenta curve, increases Z_o. Intuitively, increasing the chip pads spacing decreases the coupling capacitances but increases the mutual inductance. Hence the increase in Z_o. A similar argument can be said about the other case

when the radius is fixed at 15μm. Increasing the pad spacing from 50μm, green curve, to 200μm, red curve, increases Z_o.

For a constant chip pad spacing, increasing the BW radius from 10μm to 15μm decreases Z_o along the whole path. For example, when keeping chip pad spacing constant at 50μm, changing the BW radius from 10μm, blue curve, to 15μm, green curve, decreases Z_o by about 25Ω. Intuitively, increasing the BW radius increases the coupling capacitances but decreases the mutual inductance. Hence the decrease in Z_o. A similar argument can be said about the other case when the chip pad spacing is fixed at 200μm. Increasing the BW radius from 10μm, magenta curve, to 15μm, red curve, decreases Z_o by about 25Ω.

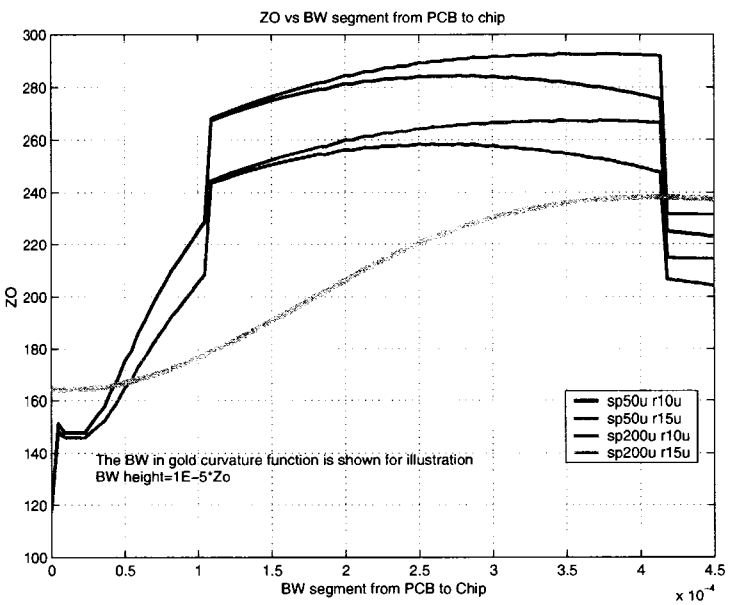

Figure 6.8 Z_o for chip on board assembly

Figure 6.9 represents Z_{odd} and Z_{even} of the BW design example. Z_{even} is usually greater than Z_{odd} due to the increase in capacitance, and decrease in inductance in Z_{odd}. Varying the chip pad spacing and BW radius leads to a similar behavior to Z_o in Figure 6.8.

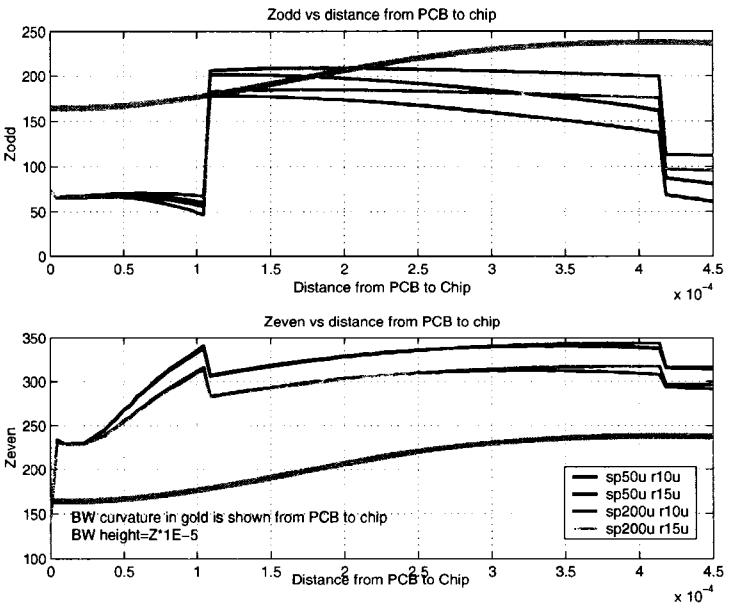

Figure 6.9 Z_{odd}, Z_{even} for chip on board assembly

6.9 Design example for modified Chip on Board

In Figure 6.1 the chip surface is not at the same level as the PCB metal level. If the chip level is the same as the PCB metal layer, then Z_o can be expected to be flat along the BW path, and less discontinuity is observed. Figure 6.10 shows a modification of the COB assembly where the dielectric of the PCB is removed under the chip. The level of the chip is made to be the same as the PCB metal layer.

Figure 6.11 and Figure 6.12 represent Z_o, and Z_{even} and Z_{odd}, respectively. Note that Z_{even} is almost constant along the path of the BW except at the ends. If the BW height above the dielectric material is constant, and the chip pad spacing is close in width to the PCB pad spacing, then Z_{even}, and Z_{odd} are almost constant along the BW path. One example is for spacing of 200μm and BW radius of 15μm and is shown in red in Figure 6.12. Table 6.3 presents the total RLGC values for this case.

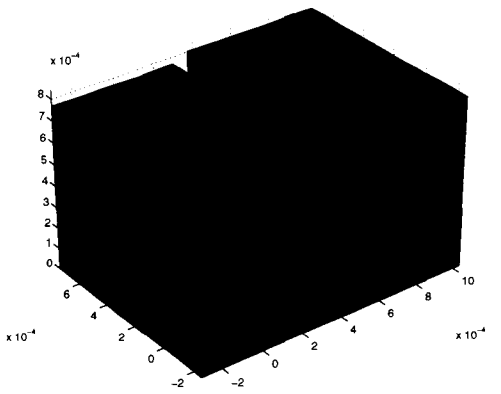

Figure 6.10 3D View of modified chip on board

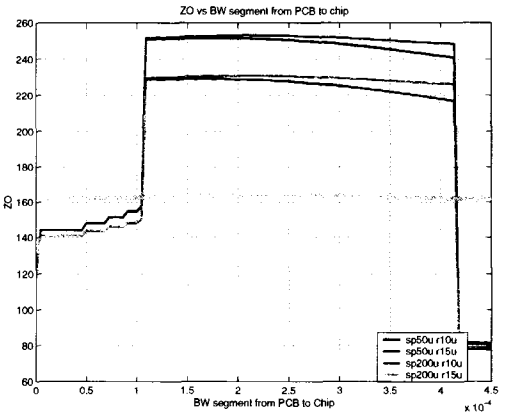

Figure 6.11 Z_o for modified chip on board assembly

6.10 Limitation of approach

Bonding wire modelling using the HSPICE Field Solver approach has some limitations. The FS in HSPICE only takes into consideration the perpendicular magnetic waves around the cross-section of the BW. The lateral magnetic fields, along the path of the BW, are not taken into consideration. This approximation holds for a few GHz frequency range. Another limitation is that the bonding wire is always assumed to have vertical cross-sections that are circular. This is an approximation in the geometry of the interconnection. The best way possible is to use a 3D electromagnetic modelling software to perform a 3D model of the

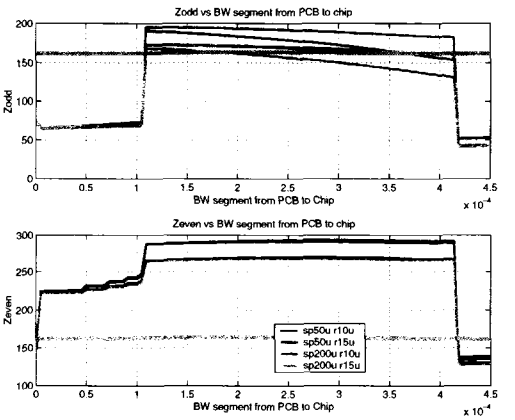

Figure 6.12 Z_{odd}, Z_{even} for modified chip on board assembly

Table 6.3 Input electrical parameters to BW toolbox

Parameter	Total value	Unit
R_o	22.8	Ω
R_f	9.9×10^{-7}	Ω
G_o	0	mho
G_f	2.44×10^{-16}	mho
C_{even}	14.96	fF
L_{even}	696	pH
C_{odd}	25.1	fF
L_{odd}	133	pH

bonding wire.

6.11 Contribution summary

In this chapter a bondwire modelling toolbox is developed for the case of Chip on Board assembly. The toolbox produces a circuit model that can be used in HSPICE simulation. The analysis shows that the level of impedance discontinuities in the BW decreases if the BW does not change the height along its path from the PCB to the chip. If the BW is flat (ribbon) then the impedance variations can be greatly reduced.

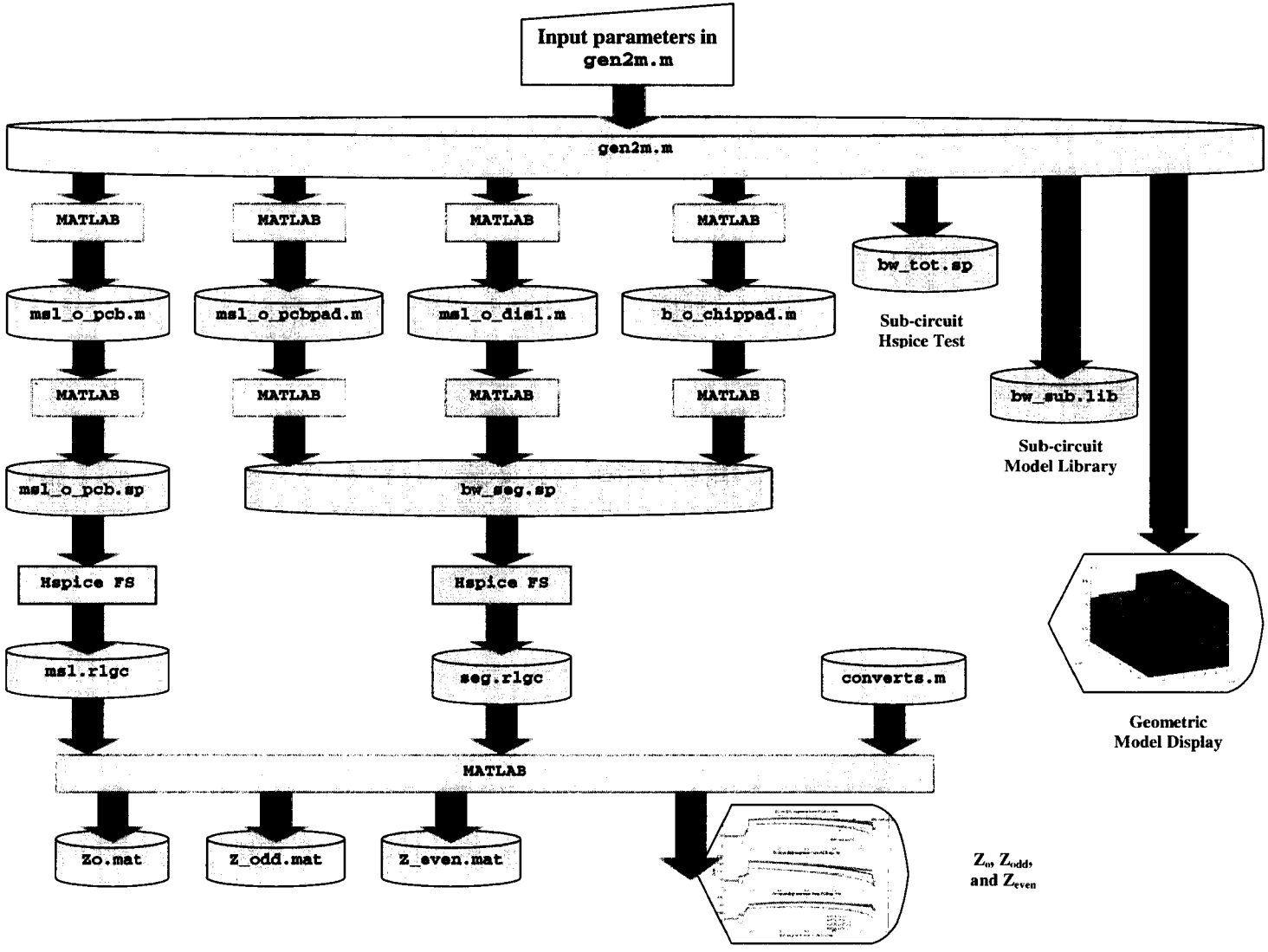

Figure 6.13 Flowchart for BW model generator `gen2m.m`

CHAPTER 7. RF and Gbit/s electrostatic discharge protection design

7.1 Introduction

In this chapter, the Electrostatic Discharge (ESD) problem is addressed in the transmitter and the receiver. The mechanism of ESD protection is to provide an alternate low impedance path for the current spark to be discharged to the substrate or ground of the chip instead of entering the internal circuitry and damaging sensitive active and passive devices.

The ESD event can be the result of human hand touching the chip or even getting close to it. The human body can be charged up to several kilo-Volts. One source of the charge accumulation is the person walking on carpet. If the human hand touches a chip already charged at a ground potential, a potential difference will result in discharge of the charge on the human body to the chip. The electrical model for this phenomenon is called the Human Body Model (HBM) [59]. This ESD event can be damaging to the chip.

Another source of ESD event is when the chip charges itself, and then discharges after one of its pins is connected to another potential point like ground. If it is not well protected, the ESD event of this type is faster and more critical to the chip than HBM phenomenon. The electrical model for this event is known as the Charge Device Model (CDM) [60].

In the normal circuit operating mode, the ESD device is off and virtually no current passes through it. The input signal bypasses the ESD device and is directed to the internal circuitry which is usually the gate of a MOSFET transistor or the base of a bipolar transistor. In principle, the ESD device should not affect the normal operation of the chip internal circuit. In reality, the ESD device does affect the electrical properties of the signal path, and careful consideration of the tradeoffs should take place to ensure the optimal performance of the chip.

In the case of an ESD event, The ESD device is activated through the voltage breakdown

characteristics of the device. The ESD device bypasses the internal circuitry, and provides an alternate low impedance path for the large current to be dissipated in it. The ESD device is designed to be large enough to be capable of passing current on the order of several Amperes. However, using a large device comes at the cost of increasing parasitic capacitances at the node where the ESD protection is introduced.

If the internal circuitry of the chip does not have ESD protection devices, then its vulnerability to ESD damage is high. If an ESD current affects the chip and passes through the internal circuitry, a damage can occur to it in the form of dielectric breakdown of gate oxide [65]. In a typical submicron CMOS process, the gate oxide material used is usually Silicon Dioxide, SiO_2, which has a dielectric strength of around $8-10MV/cm$. The thickness of SiO_2 is on the order of $40-50\mathring{A}$ in a typical CMOS process where the minimum drawn feature length is $0.18\mu m$. Therefore, if a voltage in excess of 3V is applied to the gate, it can be damaged. As a result, a voltage applied to the transistor gate of this magnitude should be prevented .

Another form of ESD damage is due to thermal damage of SiO_2 and metal interconnect. This happens because of the poor thermal conductivity of SiO_2. The I^2R heat is generated in the path that the current takes such as a metal interconnect. Since the ESD event elapses for a short time with large current, the heat is not dissipated as quickly as needed. The temperature of the SiO_2 is raised locally to a degree that the silicon is damaged and the metal interconnect is melted. A short circuit or an open circuit can occur and in many cases the damage can be seen under the microscope as a localized burn or melting of the metal interconnect. In addition, high leakage current in the ESD device can be observed after breakdown [2].

7.2 Merits of ESD protection structures

The ESD protection structure should be able to meet several goals, some of them are challenging. In many cases, there is a compromise between the high protection level, circuit operation frequency, size, and silicon area in order to achieve the best ESD protection circuit for a specific chip or design. Some of the merits of ESD protection structures are listed below [2]:

1. The ESD device should be able to shield the internal circuit from an ESD event without degrading the performance of the chip in terms of bandwidth or voltage swing. The ESD device should not act as a low pass filter limiting the maximum frequency of operation of the device, or the maximum speed of data transmitted. The parasitic capacitance of the device should be maintained at a minimum.

2. The ESD device should be able to maintain a high ESD current in the range of several Amperes and high ESD voltage, around $2 - 4kV$ or more, efficiently without damaging itself.

3. The ESD device must be reliable enough to protect the internal circuit repeatedly, and not only once, without self destruction such as melting of metal interconnect or dielectric damage.

4. The ESD device should be able to clamp the ESD voltage to safe levels for the internal circuitry.

5. The ESD device should not limit the input voltage swing of the input circuit and its trigger voltage should be above that range.

7.3 ESD devices operation

In the following sections, a brief introduction to several basic ESD devices is presented. This includes ESD diodes, Grounded Gate NMOS (ggNMOS), Gate Coupled NMOS (gCNMOS), and Silicon Controlled Rectifiers (SCR).

7.3.1 ESD Diode

The pn junction diode is the simplest ESD protection device and can operate as an ESD device in the forward bias and reverse bias mode. In the forward bias mode, the threshold voltage is around $0.5V$ [15]. it can operate as a protection device in the forward bias mode where a small voltage, $0.65V$, appears across its terminals. It has a forward bias resistance on the order of $20 - 100\Omega/\mu m$.

The forward bias current voltage relationship can be written as [62]:

$$I_D = I_s \left(e^{\frac{qV_D}{nkT}} - 1 \right) \tag{7.1}$$

where

$$I_s = Aqn_i^2 \left(\frac{D_P}{L_P N_D} - \frac{D_N}{L_N N_A} \right) \tag{7.2}$$

I_D is the current that passes through the diode. q is the electron charge, $1.602 \times 10^{-19} C$. V_D is the terminal voltage across the diode. $n = 1$. k is Boltzmann's constant, $1.38 \times 10^{-23} J/K$. T is the absolute temperature in Kelvin, $300K^{\circ}$. A is the junction size. n_i is the intrinsic concentration of electrons in the material. D_P and D_N are the diffusivities of the holes and electrons, respectively. L_P and L_N are the minority carrier diffusion lengths of holes and electrons in the n and p regions, respectively. N_D and N_A are the impurity densities of donors and acceptors, respectively.

At high currents comparable to ESD event levels, the current voltage relationship becomes [2]

$$I_{high} = I_{s2} \exp \left(\frac{qV}{2kT} \right) \tag{7.3}$$

and

$$I_{s2} = I_s \left(\frac{2N_B}{n_i} \right) \tag{7.4}$$

where the diode becomes conductively modulated. This means that both the p and n concentrations contribute to the current and both are higher than the original doping concentrations. The conductivity modulation occurs after the carrier transient time in the lower doped region is reached. At first, the series resistance of the diode is high then it becomes lower when the carrier lifetime is reached. This time can be on the order of the transient time in the CDM signal. Therefore, care should be taken to make the carrier lifetime shorter than the transient time of the CDM discharge.

In the reverse biased region, the leakage current is small and due to thermally generated carriers in the depletion region. When the reverse voltage increases, the carriers in the depletion region collide and produce electron hole pairs, and each one of them produces a set of electron-hole pairs, and so on. This phenomenon is called avalanche multiplication. At this stage, the

diode conducts large amounts of current. The threshold voltage for breakdown is [62]:

$$V_{BD} = \frac{\varepsilon_s E_{max}^2}{2qN_B} \tag{7.5}$$

where ε_s is the semiconductor permittivity, and E_{max} is the maximum electrical field in the depletion region. The avalanche multiplication factor can be empirically written as [41]:

$$M_{n,p} = \frac{I_{n,p}(out)}{I_{n,p}(in)} = \frac{1}{1 - \left(\frac{V_j}{V_{\text{av}}}\right)^n} \tag{7.6}$$

where the V_j is the junction diode potential, and V_{av} is the avalanche breakdown voltage. n is a fitting number between 2 and 6. As V_j approaches V_{av}, M becomes very high and reaches ∞.

7.3.2 ESD Grounded Gate NMOS (ggNMOS)

The NMOS transistor normal operation follows the square law model [52]. While normal NMOS transistors can carry small currents, ESD transistors are designed to pass currents in the range of several Amperes. From its name, the ggNMOS has its gate (G) and source (S) grounded. The drain (D) is connected to the node to be protected from ESD. If $V_G = 0$, and the drain voltage V_D is increased, no current passes between the drain and source till $V_D = V_{\text{av}}$ which is the avalanche voltage of the device.

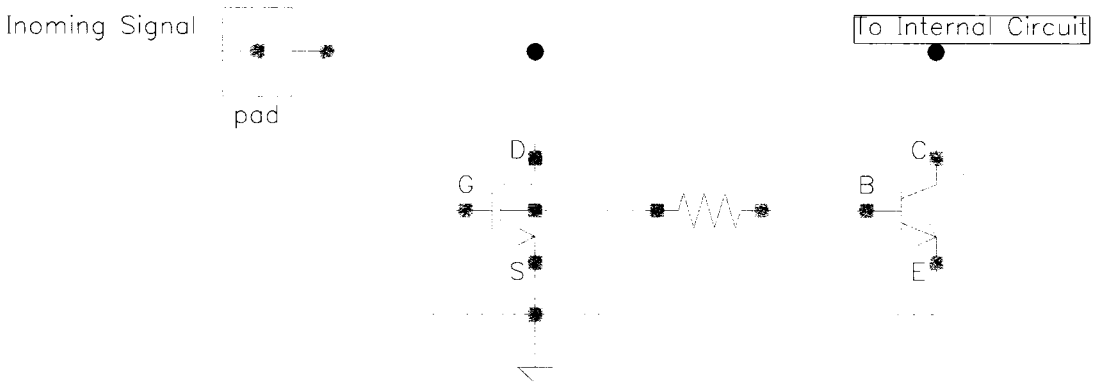

Figure 7.1 Grounded Gate NMOS with lateral bipolar NPN

The NMOS transistor has a parasitic lateral NPN bipolar transistor. The NPN collector is the NMOS drain, while the NPN emitter is the NMOS source. The NPN base is the same

as the NMOS substrate. The substrate resistance can be seen as being connected to the base of the NPN. A schematic is shown in Figure. 7.1. As for operation of the device, the drain current is first negligible. As V_D is increased, the reverse biased drain substrate junction observes an increase in the number of electrons entering the drain from the substrate and the number of holes entering the substrate from the drain, due to impact ionization, giving rise to substrate current, I_{sub}. I_{sub} passes from the emitter to the substrate and through the substrate resistance. When V_{B} becomes higher than V_E by approximately $0.5V$, the lateral NPN is turned on and more electron hole pairs are generated. This turn on voltage happens at $V_D = V_{\text{t1}}$ and the corresponding $I_D = I_{\text{t1}}$. It was shown that for a $1\mu m$, channel length, the turn on time is on the order of $250ps$ [36]. After turn on, V_D decreases, due to the availability of I_C till a minimum voltage V_{sp} is reached. The resistance is increased again because of the decrease of substrate resistance R_{sub} due to conductivity modulation [2]. Another breakpoint V_{t2} is reached where a thermal failure affects the transistor.

7.3.3 ESD Gate Coupled NMOS (gCNMOS)

It is very desirable that $V_{t1} < V_{t2}$ which means that the avalanche breakdown happens before the thermal breakdown of the device. This is important when the ESD device is designed as a multi-fingered structure; i.e. as a set of NMOS transistors connected in parallel. The gCNMOS consists of an NMOS device, a capacitor and a resistor. The capacitor C is connected between the gate and drain, while the resistor R is connected between the gate and ground. The bulk of the transistor is connected to ground while the drain is connected to the node where ESD protection is introduced. [20]. A schematic is shown in Figure 7.2.

As for the ggNMOS, I_{sub}, is responsible for turning on the lateral parasitic NPN bipolar transistor of the gCNMOS. Since the RC path increases I_{sub}, less I_{sub} is needed from avalanche multiplications to turn on the transistor. Therefore, R and C are chosen such that V_{t1} can be lowered. This is a useful method for turning on the NMOS transistor for less voltage and in a faster way than the ggNMOS case.

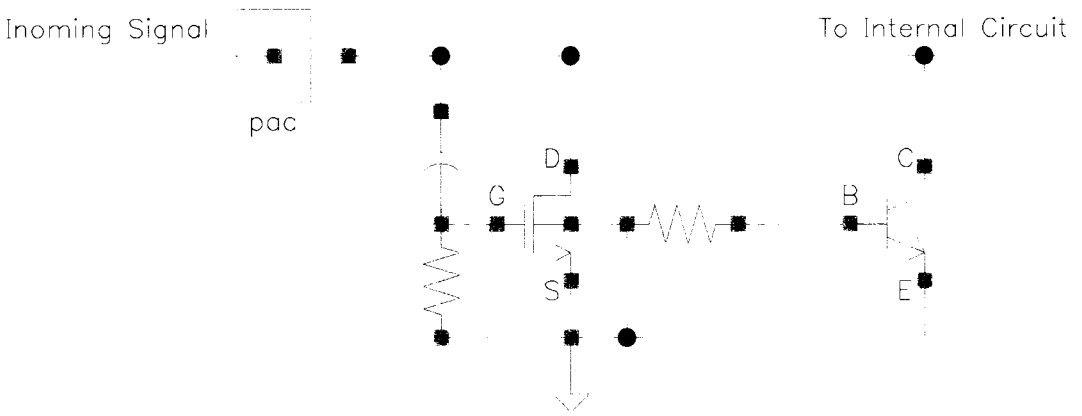

Figure 7.2 Gate Coupled NMOS with lateral bipolar NPN

7.3.4 ESD Silicon Controlled Rectifier (SCR)

The SCR device can be seen through the latch-up process that affects digital circuits manufactured on high resistivity substrates. As an example, a CMOS inverter consisting of an NMOS and PMOS transistors are drawn close to each other where the PMOS is placed in an N-WELL, is considered. The NMOS transistor has a parasitic lateral bipolar NPN transistor, while the PMOS has a parasitic vertical bipolar PNP. The NPN base is the N^+ of the substrate through the substrate resistance. The NPN emitter is the NMOS source, and the collector is the n-well. As for the PNP, its base is connected to the well's P^+, the emitter to the PMOS source, while the collector is connected to the p-substrate. The anode of the SCR is the PNP emitter, while the cathode is the NPN emitter. The n-well substrate and PNP source are connected to power supply while the p-substrate and NPN source are connected to ground [2].

In the case of an ESD event, the SCR is turned on when the anode to cathode voltage exceeds the breakdown voltage of the PN junctions at the collectors of the NPN and PNP. When the transistors turn on, they provide the current for themselves, and a negative resistance effect is observed. As a result, the anode to cathode voltage drops and the ESD node shunts to a low voltage V_{h}.

7.4 Types of ESD protection

There are several types of ESD protection structures depending on the purpose of the protection. Such ESD structures are implemented for power supply, input/output, and RF and Gbit/s circuit. Below is a brief description of each type.

7.4.1 Power supply ESD protection

In the case of a power bus protection, a grounded gate NMOS (ggNMOS) transistor can be used as a power supply clamp [65]. It provides a low impedance path between the power line and ground in the case of an ESD event affecting the power line. The gate and source of the NMOS are connected to ground while the drain is connected to the power line. The ggNMOS is OFF in normal operation. When activated, it shunts the power line to ground discharging the ESD current to GND without raising the supply voltage of the circuit to damaging levels. Another implementation of an ESD power clamp is through a set of diodes forward biased and connected in series [15]. The Darlington effect, which is the reduction of the diode voltage across the diode string due to lower current densities in later stages, limits the number of diodes that can be effectively connected in series. This effect can be eliminated by adding a bias network that adds a small current to the diodes across the string to bias them. A variation of this scheme is to add an SCR to the diode string as in [34] to lower the leakage current in the diode string.

7.4.2 Input/Output ESD protection

Another ESD protection type is for input/output circuits. In a line driver protection, the output pads are usually connected directly to the driver NMOS and/or PMOS drains. The ESD protection circuit is connected between the output pad and ground (GND). Another ESD device is placed between the output pad and the power supply line (Vdd). The purpose of these two circuits is to provide a low impedance path to a power supply in the case of a positive or negative ESD signal affecting the chip.

Typically, a combination of diodes, ggNMOS, ggPMOS, and/or SCR devices can be used

as protection devices [64]. A similar approach can be implemented in the case of an input protection circuit. In order to reduce the trigger voltage of the input ESD device, a gate coupling NMOS (gCNMOS) is used [15]. The gCNMOS consists of an NMOS, a capacitor between the gate and drain, and a resistor between the gate and ground. The drain is connected to the input node.

7.4.3 RF and Gbit/s circuit ESD protection and challenges

The problem of ESD protection for RF and very high speed circuits is a challenging task. The challenge is in designing an ESD protection structure that is capable of at least Class 2 (2kV-4kV) [59] level of protection. At the same time, it does not impede signals with high frequency content in the GHz range, and should turn on faster than the internal circuitry in order to achieve protection. In addition, it should be able to meet the ESD merits in Section 7.2.

One challenge in RF ESD design is the accidental turn on of an ESD device even before avalanche breakdown happens. [5] and [65] show a correlation between the ESD trigger time V_{t1} and the rise time of the input signal t_r. In other words, the high dV/dt rate in the signal that passes through the ESD protection node can accidentally trigger the ESD device to turn on even below the original designed V_{t1} level. For a reverse biased PN junction, in a ggNMOS for example, the capacitance is high. Since the current equation for a capacitor is $i(t) = CdV/dt$, $i(t)$ can become high. This current can pass through the base of the lateral NPN to raise the base voltage, and turn on the NPN before avalanche breakdown happens. This can be catastrophic for an RF or high speed IC since it will create a short circuit at the input and no signal can enter the chip.

For an NRZ signal with a maximum data rate of 10 Gbit/s, the bit period T_{bit} is 100 ps. The rise time t_r is about $30 - 50$ ps. Let the voltage swing be 400 mV. This means that

$$\frac{dV}{dt} = \frac{400 \text{ mV}}{30 \text{ ps}} = 1.33 \times 10^{10} \text{ V/s} \tag{7.7}$$

In order to avoid this accidental triggering, dV/dt is designed to be less than the ESD

triggering rate. However, this is not an option in RF circuits or in Gbit/s rate integrated circuits.

Another suggestion is to decrease the reverse biased junction capacitance of the drain of the ggNMOS. The cost of that is the inability to pass high ESD current because of the drain small size. As a consequence, the ESD protection level is lowered to levels, sometimes on the order of several hundred volts, as opposed to several kV protection in low speed chips. In some other circuits, the ESD is removed altogether and require an ESD free handling, assembly and testing environment. If extreme care is not provided in maintaining an ESD free environment, the chip yield is to be sacrificed since a large percentage of the chips are very vulnerable to ESD phenomena and many of them are prone to be damaged even by being close to a charged body. They can be self charged and destruct themselves by discharging.

Diodes can be optimized to be included as ESD devices in RF ESD protection [53]. The diode layout is the same as an NMOS with the source connected to the substrate through P^+. Two diodes are used to connect to Vdd and GND from the pad. They are forward biased in the case of an ESD event. The resistance along the ESD current path is minimized too. In [53], the diode network provides protection of 2 kV HBM with a maximum parasitic capacitance of 150 fF per pin. If the pad parasitic capacitance, for a typical $75\mu \times 75\mu$ pad, is around 25 fF, the total capacitance is around 175 fF per I/O pad.

In [25], an SCR device is suggested as an ESD device. The device provides protection for a positive ESD pulse and a negative ESD pulse to Vdd and GND. The device parasitic capacitance is around 90 fF for a $4kV$ HBM ESD voltage. Copper is used as the interconnect metal layer instead of Aluminum because it can withstand more current, and therefore it can provide the same toughness for less parasitic to GND. The use of SCR in RF circuits is subject to the latch-up problem. This means that the ESD device may trigger and latch at a low impedance point in normal circuit operation and basically shorts the input node to ground. The device may accidentally trigger at high frequencies because of the dV/dt problem. If pads are considered, the total parasitic capacitance is 115 fF per pin.

About [53], and [25], the following observations can be made:

1. Both approaches mention protection measured using the HBM model which is less severe than subjecting the model to the CDM test. The CDM test has considerable signal frequency content that can reach 1 GHz, and a rise time that is very short, on the order of less than 1 ns.

2. The ESD protection approaches rely on the input signal being directly connected to the internal circuitry, and the ESD device protects it by diverting the ESD signal away from reaching internal circuitry. It is highly desirable to have the internal circuitry completely isolated from the outside world. In this case, the ESD event signal and the input data (or information) signal are isolated from the internal circuitry. Any transfer of data or information is done through capacitive or inductive coupling.

The ESD isolation method for RF and Gbit/s circuits is the focus of the research in this dissertation.

7.5 Thesis ESD protection design objective

One of the objectives in this dissertation to develop an improved ESD protection scheme for RF and Gbit/s integrated circuits that has the following characteristics:

1. The ESD structure should be able to protect the internal circuitry from high ESD transients, preferably Class 2 (2-4 kV) HBM and CDM.

2. The ESD structure should have the minimum parasitic capacitance that can load the internal circuitry.

3. The chip should be able to send and receive data up to 10 Gbit/s and frequency range of more than 5 GHz without being impeded by the parasitic capacitances.

4. The internal circuitry is completely isolated from the outside world. This means that there is no direct wire connection from outside the chip to internal circuitry.

5. The ESD structure should be reliable and withstand repeated ESD events effectively.

6. The structure is simple to design, layout and fabricate.

Section 7.6 describes the new proposed ESD protection scheme contributed in this thesis work.

7.6 Proposed ESD protection structure

Figure 7.3 presents the proposed RF ESD protection scheme. It consists of the following

1. Two identical monolithic transformers

2. An ESD device connected between the transformers

3. Spark gaps placed close to the pads

The monolithic transformers are designed on-chip. They should operate as transformers up to 6 GHz minimum. The ESD device connected in the middle can be a set of diodes that operate in forward bias in the case of and ESD event. An SCR can be a choice too. It is important to observe that the middle point between the transformers is balanced and therefore can be considered as an AC ground. This is due to the fact that the signal transmitted is differential. The parasitic capacitance of the ESD device in the middle does not affect the normal circuit operation. As for the spark gaps, they are special devices fabricated in a standard CMOS process, and ignite and form a low impedance to ground during an ESD event.

This ESD scheme is included in a 10 Gbit/s wireline data driver. It can be incorporated into the receiver too. Another application is RF circuits such as the input node to a Low Noise Amplifier (LNA).

In section 7.6.1, and 7.6.2 an introduction is given to spark gaps and field emission devices. Section 7.6.3 presents a more detailed description of the proposed ESD structure.

7.6.1 Characteristics and operation of spark gaps

The spark gaps implementation as ESD devices is not a new idea. They were used as over-voltage protection devices in telephone installations long time ago [61]. The spark gaps

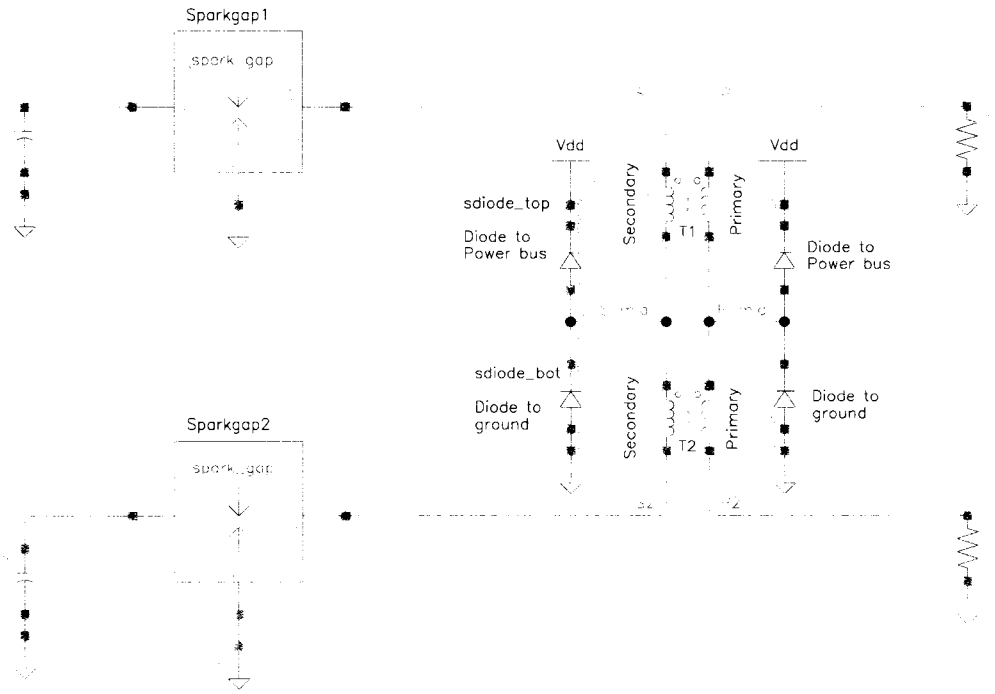

Figure 7.3 Driver ESD structure schematic with spark gaps

work on the principle that if a large electrical field exists between two points, the accumulation of large positive charge on one point and large negative charge on the other node ionizes the air or the medium between them to the degree that the ionized air becomes conductive and a flow of electrons passes from one of the points to the other. The current flow takes the shape of an arc or a spark, hence the name arc gap, or spark gap. The following observations about spark gaps are listed below:

1. The spark initiation delay time is defined as the time elapsed from the peak of the ESD event current signal to the peak of the spark gap current signal. It is largely dependent on the parasitic capacitance associated with the gap [63]. If the capacitance between the anode and the cathode of the gap is low, and the self capacitance of the anode to ground, and cathode to ground is low, the initiation delay time can be kept as a minimum. This can be shorter than the rise time of the CDM signal.

2. In [12], page 195, it is stated that the avalanche initiation ions can travel the distance

of the arc gap with the speed of light. This is, of course, provided negligible capacitance effect exists across the gap. it can be assumed that the initiation delay-time is dominated by the parasitic effects, but not the avalanche-initiation phenomena.

3. The luminous front of the spark in the spark gap travels at a velocity up to 3×10^7 cm/s [66]. Therefore, for a typical spark gap of around 3μm, the travel time from the start to the end of the gap is about 10 ps.

4. The arc channel radius can be calculated according to [8], as

$$R = 0.93 \frac{\sqrt[3]{I}\sqrt{t}}{\sqrt[6]{\rho}} \tag{7.8}$$

Where ρ is the density of air at atmospheric pressure 1.29×10^{-3}g/cm^3, I is current in kilo-ampere, and t is time in microseconds. This would approximately give an arc channel of radius in the order of a 1×10^{-9} m.

5. Although [40] reported a shorting problem with spark gap devices with gap spacing less than 25μm (0.4um aluminum thickness), this happened with a gap of only less than 3 microns (3um Aluminum thickness) in [63]. Several factors affect the minimum gap spacing such as the process used, the metal type (Aluminum was used here), and the metal thickness chosen.

6. The electrical model of the arc channel can be scaled from [27] and presented as a series combination of around 0.02 ohm and .5 nH for a 3μ m.

7. The spark gaps assume a 45 degree saw tooth shape [13] with several teeth. It was shown that it provides higher reproducibility than flat parallel shapes [48][29], or 90 degree shapes [13]. In addition, sawtooth interdigitaed arc gap structures show better reliability than point to point sawtooth structures [28]. On the other hand, it was reported by [47] that parallel plate spark gaps can provide good protection for the circuit where polysilicon material was used instead of high conductivity metal.

8. The average breakdown voltage for metal to metal gap spacing of 3um is around 250V for passivated gap, while it was around 175V for an unpassivated gap [13], while the voltage across the arc is in the order of 20V when the arc is present.

9. The Aluminum or Copper metal that is used to build the spark gap can be replaced by a higher resistivity material such as polysilicon. The advantage of polysilicon is that it greatly reduces the melting and shortening of the metal when a spark occurs. Thus the reliability of the spark gap can be increased [46]. Another advantage is the ability to reduce the gap spacing and trigger voltage. This leads also to a faster response.

7.6.2 Field emission devices

The spark gaps usually depend on high electric field to ionize the atoms and molecules to form a discharge path along the gap. There is a considerable amount of heat is generated from the spark gaps when ignition is initiated. Another method of current discharge is *field emission.* Field emission happens when an a metal material is adjacent to a semiconductor material. The potential barrier for the electron in metal to overcome is much smaller than the potential barrier of metal to vacuum. If the distance, horizontally, or vertically, between two metal layers is small, on the order of tenths of a micron, electrons tunnel through the semiconductor and reach the other metal edge. This is called Field Emission. It occurs when the electrical field is on the order of $0.5V/\mathring{A}$ [9]. If protection to the circuit is needed to be around $10V$ for example, then a semiconductor gap on the order of $20\mathring{A}$ needs to be fabricated. Special fabrication techniques are suggested by [38]:

1. In the first method, a first metal layer (M1) of thickness (T1)is deposited over the field oxide (FOX). The field oxide is etched to the thickness of T1 *below* M1. Thus the base of M1 is raised above FOX by T1. The etching might go for a small distance underneath M1. A second metal layer M2 is deposited. M2 is deposited on two levels; on M1 and on the field oxide. If the process is calibrated well and the thickness of M2 is calculated accurately, then there is a small area between M1 and M2 on the lower FOX layer that is very small in the order of few nanometers. A dielectric material deposited above the

whole structure seals the cavity and if this is done in vacuum, the gap is vacuumed. The edge of M1 and lower M2 can extend to a long range to make a wedge.

2. The other method is to deposit a metal layer M1 on the substrate. Then a dielectric material is deposited on it leaving a gap of size R. Another dielectric material is deposited again leaving the same gap R. A third dielectric material is deposited on the whole structure including the gap creating a valley with a pinpoint in the gap R. Above that a metal M2 layer is deposited above the whole structure including the gap to form a metal pinpoint at the bottom of the valley. M2 is now the cathode that generates the electrons and the anode is M1. This can be on the form of a wedge. Several wedges can be connected in parallel.

An inverted method where a small wedge with a pin tip on the top as the cathode and the anode is above it is cited in [26]. The metal cathode can be made from semiconductor material that has a thin layer of metal deposited on it [7]. This method increases the resistance of the cathode since the maximum current can be controlled in the semiconductor by doping. If more current is affecting the wedge, the electrical field decreases and the current is diverted to other areas of the wedge [7].

7.6.3 Description and layout

7.6.3.1 Transformers

The transformers in Figure 7.3 are connected in series. The two ports of the primary are connected to the internal circuitry and the two ports of the secondary are connected to the bonding pads. The transformer layout can be planar interleaved, planar concentric, or toroidal solenoid (this can be fabricated when the process can be customized to have a thick dielectric material). A patent [21] describes an inductor layout where the magnetic flux leaving the center of the first inductor, enters the center of a second inductor. When connected together, both inductors form a single inductor where the flux is contained inside its elements and forms a loop. This method can be extended to lay out two transformers that form one transformer with the flux contained in it.

7.6.3.2 ESD protection structure

On the secondary side, in the middle point between the transformers, an ESD protection circuit is placed and consists of a protection circuit to ground like a diode. The anode is connected to ground while the cathode is connected to the ESD node. An additional protection circuit to Vdd such as a diode can also be used. The second diode's anode is connected to the ESD node, while the cathode is connected to Vdd. This configuration is necessary in order to protect against both positive and negative ESD signals. The middle point between both transformers is always balanced during operation and can be considered to be AC ground. Therefore, the ESD structures (to GND or to Vdd) in the middle do not affect the circuit operation. The ESD devices can be large and have considerably large parasitic capacitances.

7.6.3.3 Spark gaps

The spark gaps are placed close to the bonding pads and on both sides of the secondary. The spark gaps can have a saw tooth shape of 45 degrees with 3μm spacing. Another implementation is to have the spark gap plates parallel to each other and have them made of polysilicon material which limits the amount of current in them and makes the spark gap ignite in more than one point. The advantage of this structure is to have a narrow gap between the anode and cathode and this makes the ignition threshold voltage smaller. The capacitance between the gap anode and cathode is kept less than 2 fF and the capacitance of the anode to GND and cathode less than 2 fF. The capacitive loading effect is minimal on the operation of the spark gap. If the height h of the polysilicon layer is known, then the ratio of the gap's vertical plate length L_{gap} to the gap horizontal spacing S_{gap} is the design parameter where

$$\frac{L_{\text{gap}}}{S_{\text{gap}}} = \frac{C_{\text{gap}}}{\varepsilon h} \tag{7.9}$$

This ratio can be around 50.

7.6.4 Spark gap electrical model

The electrical model of the spark gap was compiled from different sources to reflect the electrical behavior of the phenomenon as shown in Figure 7.4 and a symbol view in Figure 7.5. The elements are:

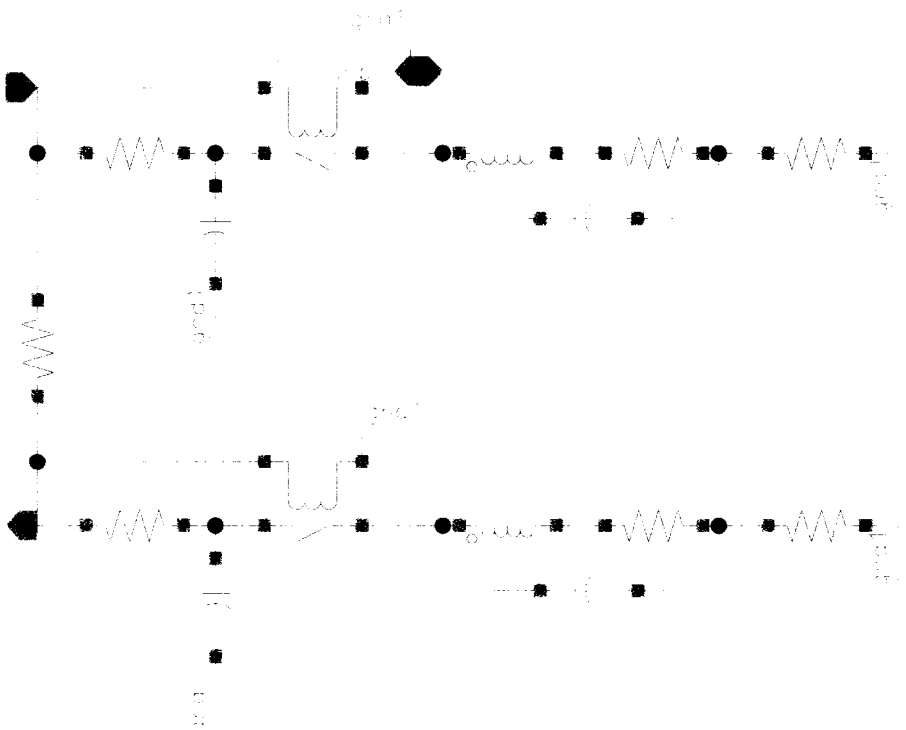

Figure 7.4 Spark gap electrical model

1. A switch closes when the voltage across the gap is about 300 V. The closed voltage is around 20 V depending on the current across it. The close voltage can be represented by a diode with this voltage.

2. A resistance of $R_{\text{spark}} = 20\,m\Omega$ in series with an inductance of $L_{\text{spark}} = 0.5$ nH, both are connected in series with the switch

3. A capacitor from the cathode to ground represents the self parasitic capacitance of the cathode $C_{\text{cathode}} < 2$ fF.

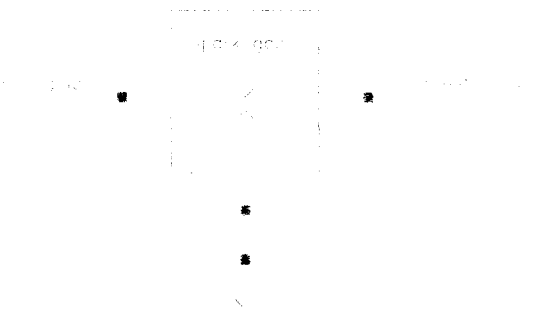

Figure 7.5 Spark gap symbolic view

4. A capacitor from the cathode to anode represents the coupling capacitance of the cathode in the range of $C_{\text{anode}} < 2$ fF.

5. The cathode is connected to the node where ESD protection needs to be introduced. The anode is connected to ground

6. To model the effect of a negative ESD event, the whole structure is repeated except that the closing voltage of the switch is negative this time.

7.7 Mode of operation of the proposed ESD structure

7.7.1 Normal mode of operation

In the normal operation mode, the transformers, center ESD structure, and spark gaps act as part of the driver circuit in a wireline data communication serializer and deserializer scheme. The signals enter the transformer primary in differential current mode fashion. The four port transformer acts as an isolator. With a low cutoff frequency of 1.5 GHz, the transformer attenuates any frequency components of the input signal below that frequency range. In the differential input to differential output mode, the resonance frequency is 6 GHz. The transformer has a capacitance of 44 fF to ground. The mutual coupling capacitance between the primary and the secondary is around 40 fF. The secondary of the transformer shows an induced voltage depending on the time change of the input current signal dI_{primary}/dt and the amount of mutual inductive coupling between the primary and secondary M. In

the frequency domain, where the current signal can be written as a fourier series of all the frequency components of the signal,the induced voltage to input current relationship can be expressed as $j2\pi fM$, where f is the frequency of each signal component.

Since the input signal and the output signal are differential, the voltage at the middle points between the two transformers at the primary and the secondary remain essentially constant. The voltage at those points does not substantially change as considerably compared to the input/output pads in current ESD scheme where the ESD node changes according to the input/output signal. The transformer was fabricated in a typical 0.18μ process. The transformer is symmetric and has a common mode to differential mode $CMRR = 40$ dB up to 6 GHz. The effect of the differential input signal at the primary, on the ESD node at the secondary, is very low. Therefore the accidental triggering of the ESD node does not happen for a normal range of input signal and the differential mode of operation.

The spark gaps have less than 2 fF capacitance to ground at both ports of the primary. Their effect on the normal circuit operation is minimal because the capacitance is very small. They act as open circuit to normal circuit operation.

The total capacitance seen by the signal at the secondary of the transformer at each port is the sum of the transformer self capacitance 44 fF and the spark gap capacitance of 2 fF. This is around 46 fF per pin. If the bonding pad capacitance of 25 fF is included the total capacitance in the signal path is less than 71 fF.

The bonding pads are fabricated using only the highest metal layers to reduce self capacitance to ground. If the bonding pads are excluded, the structure in [53] has 150 fF, and the structure in [25] has 90 fF. The proposed structure in this research has about 46 fF while providing physical isolation of the signal from the outside world. The ESD structure in this research can be large and yet fast enough to withstand high current and fast triggering. The voltage protection level can be high.

7.7.2 ESD mode of operation

If any secondary port of the transformer is subjected to an ESD event, then there are three different paths for the current to flow through thus avoiding being transferred to the primary of the driver and thus to internal circuitry. The paths are:

1. Through the spark gap of the port closer to the ESD event, and to a lesser extent, the spark gap connected to the other port of the secondary. In that case, the current has to pass through the secondary windings of both transformers.

2. Through the ESD structure in the middle between the two transformers. Note that the middle point is not anymore a balanced point since the ESD event is occurring at only one port.

3. Through the secondary windings of both transformers to the other port of the transformer, and off the chip.

The turn-on time for the ESD device depends on how fast the device turns on. A typical turn-on time is on the order of 250 ps. The spark gap initiation time is about 10 ps. The time elapsed for the current signal to travel through the secondary windings of both transformers is about 40 ps. This time can be calculated assuming the transformer acts as a transmission line , in addition to the time delay caused by the ohmic resistance of the transformer windings, 20Ω and the transformer parasitic capacitances around 100 fF.

The HBM ESD event takes about 150 ns, with a rise time on the order of 10 ns. The spark gap initiates first. The current passes through the secondary windings and discharges through the other pad. When the current reaches the center ESD structure, the device turns on after about 250 ps. In essence, there are three paths for current discharge.

The transformer lower cutoff frequency is about 1-2 GHz. This happens to be beneficial in the case of an ESD event. The frequency spectrum of an HBM test signal is well below 1GHz. The transformer provides isolation and very small induced voltage is seen at the primary as a result of the ESD event at the secondary.

As for the CDM test signal, the frequency spectrum is around 1-2 GHz. The CDM event transient lasts for several 10×10^{-9}'s with a rise time less then 1 ns. If spark gaps or center ESD structures are not present, the ESD current in the secondary induces a large voltage in the primary that can be damaging to the sensitive transistor drains. This voltage can be much larger than the thermal breakdown voltage of the drain to bulk junction, and can easily destroy these devices. Consequently, it is important that the spark gaps and the center ESD structures turn on fast and effectively discharge the current. The spark gaps in this case turn on after around 10 ps, and provides a discharge path for a considerable percentage of the current before it reaches the transformer and induces a large voltage in the secondary.

7.8 ESD simulations

Two standardized test are performed on the proposed structure. The first is the HBM [59] test. The faster and more severe test is the CDM [60] test. The transformers were previously fabricated in a typical CMOS 0.18μ process. The four port characterization parameters were used in the simulations.

For each test, two simulation cases were performed. They are:

1. The transformers alone acting as ESD devices.

2. The transformers, in addition to the spark gaps and center ESD devices chosen as diodes forward biased in the ESD mode of operation.

7.9 Human Body Model (HBM) Test

7.9.1 HBM test for an ESD structure without spark gaps

The HBM simulation setup network consists of a 100 pF capacitor, a 15 uH inductor, and a $1500\,\Omega$ resistor. This test is applied to one of the input pads of the transformer secondary. The other input pad of the transformer secondary is left open as in Figure 7.6[1]. A 50 termination

[1]The following abbreviations are always associated with figures

- *L* means *L*eft, and *R* means *R*ight

resistor is placed at each transformer primary port. The ESD structure does not have the spark gaps included.

The ESD voltage VESD is displayed in Figure 7.7L. Figure 7.7R is the ESD current resulting from the discharge of the ESD capacitor. The current and voltage show a damped response due to the large ESD resistance 1500 Ω.

The transformer differential secondary voltage, $V_{secondary\_diff} = V_{S1} - V_{S2}$, Figure 7.8$UL$ raises in a damped response to more than 200 V. The transformer differential primary voltage, $V_{primary\_diff} = V_{P1} - V_{P2}$, Figure 7.8$UR$, shows peaks at 1.2 V and −0.7 V. This voltage is below the breakdown voltage, 2×4 V, of the NMOS differential pair transistors drains connected to it. This shows that the ESD structure provides protection to the internal circuit against voltages up to 10 kV. The frequency spectrum of $V_{secondary\_diff}$ ($V_{secondary\_dft}$) in Figure 7.8 LL shows that the frequency components decrease rapidly after 500 MHz. This is a nature of the HBM ESD signal. Due to the low cutoff frequency of the transformer at 1.5 GHz, the transformer attenuates the frequency components of the signal below the cutoff frequency. The frequency spectrum of $V_{primary\_diff}$, ($V_{primary\_dft}$) shows attenuation in its magnitude as in Figure 7.8LR.

Figure 7.9UL& UR shows the transformer secondary voltages V_{S1}, andV_{S2}, respectively. The response is damped, and settles down after 800 ns. The transformer primary voltages V_{P1}, andV_{P2} are displayed in Figure 7.9 UL& LL, respectively. V_{P1} shows a maximum magnitude of 1.1 V, while V_{P2} shows a maximum magnitude of 1 V. The voltage transient lies comfortably below the 4V limit for each NMOS transistor connected to each port of the transformer primary.

Figure 7.10 displays the current waveforms of the transformer secondary. Figure 7.10UL is the ESD current that enters the secondary. The peak current is 5.5 A. S_{mid} in Figure 7.10UR is the transformer secondary center point voltage. It rises to 9 V. Because $S_{mid} > V_{dd} + V_{t_{diode}}$, the top secondary diode in Figure 7.6LL is forward biased and conducts most of the ESD

- UL means *U*pper *L*eft, and UR means *U*pper *R*ight
- LL means *L*ower *L*eft, and LR means *L*ower *R*ight

current. The bottom secondary current is off as in Figure 7.6LL. Another indication that most of the ESD current is dissipated in the diodes is the transformer T2 secondary current in Figure 7.6LR. The magnitude of the current is about 6 mA. This is about 0.1% of the original ESD current.

Figure 7.10 shows the current waveforms of the transformer primary. P_{mid} in Figure 7.10UR is the transformer secondary center point voltage. Figure 7.10UL is the ESD current that enters the primary. The negative current means that it is leaving the primary. The peak current is -23 mA. P_{mid} in Figure 7.10UR is the transformer primary center point. It rises to only 1 V which is not enough to forward bias any of the primary diodes. There is a transient current in the primary top and bottom diodes due to charging and discharging the parasitic capacitances associated with the diodes junctions as shown in Figure 7.11LL. The rest of the current flows through the transformer T2 windings as shown in Figure 7.11LR.

As a conclusion, the ESD structure is able to protect the circuit against an HBM ESD event up to 10 kV. It should be noted that simulation shows that there is enough room to protect the circuit up to a higher voltage.

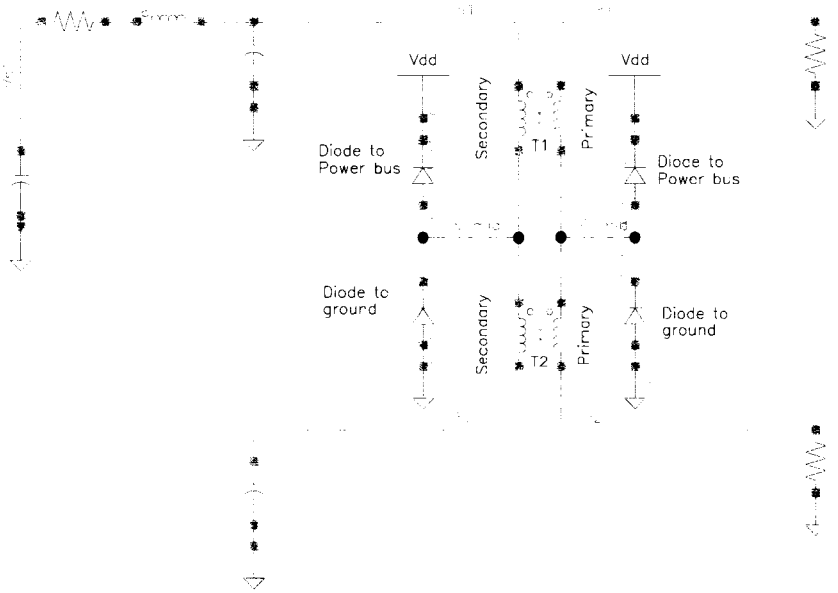

Figure 7.6 HBM without spark gaps: Schematic

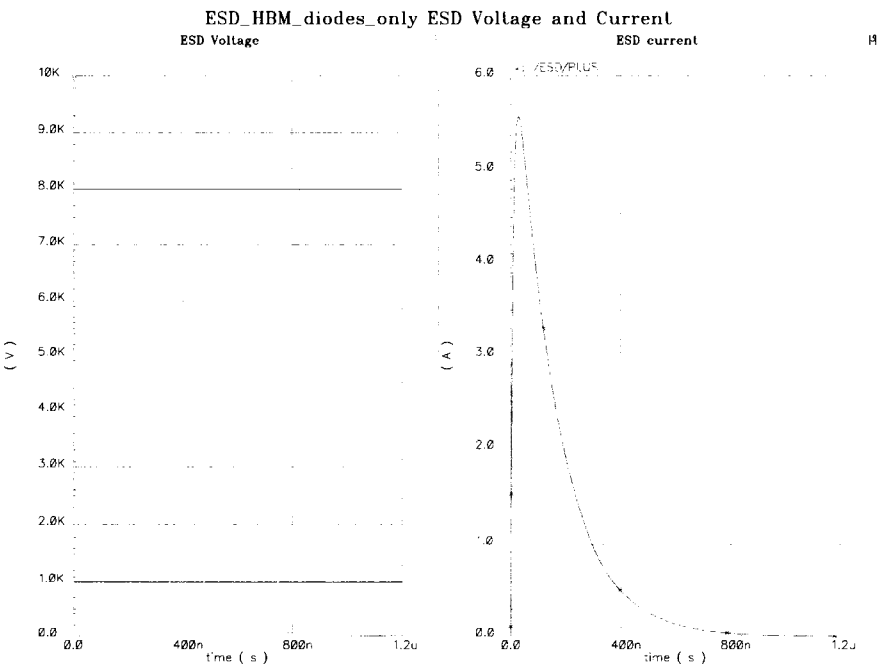

Figure 7.7 HBM without spark gaps: ESD current and voltage

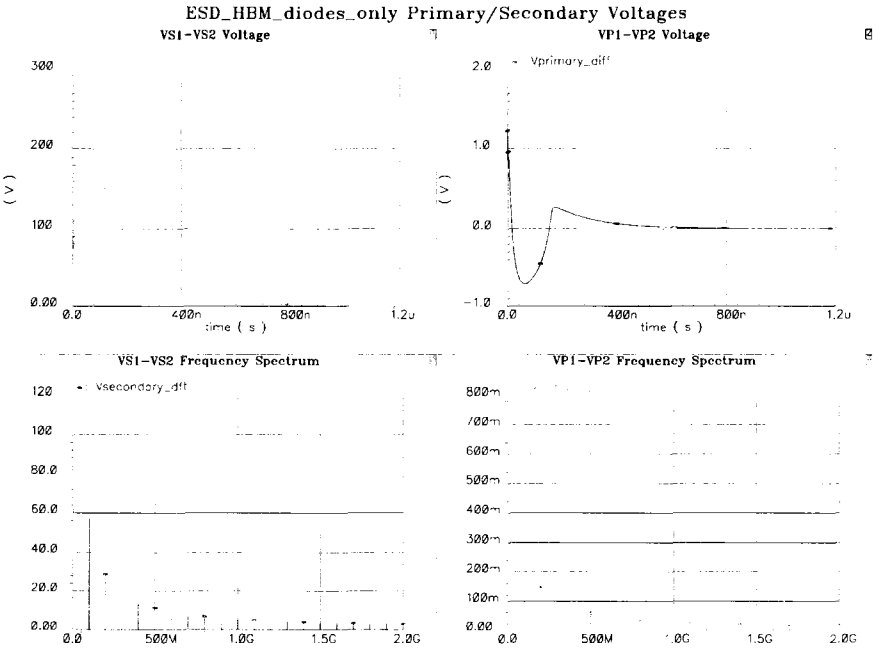

Figure 7.8 HBM without spark gaps: Sec. and Pri. voltages

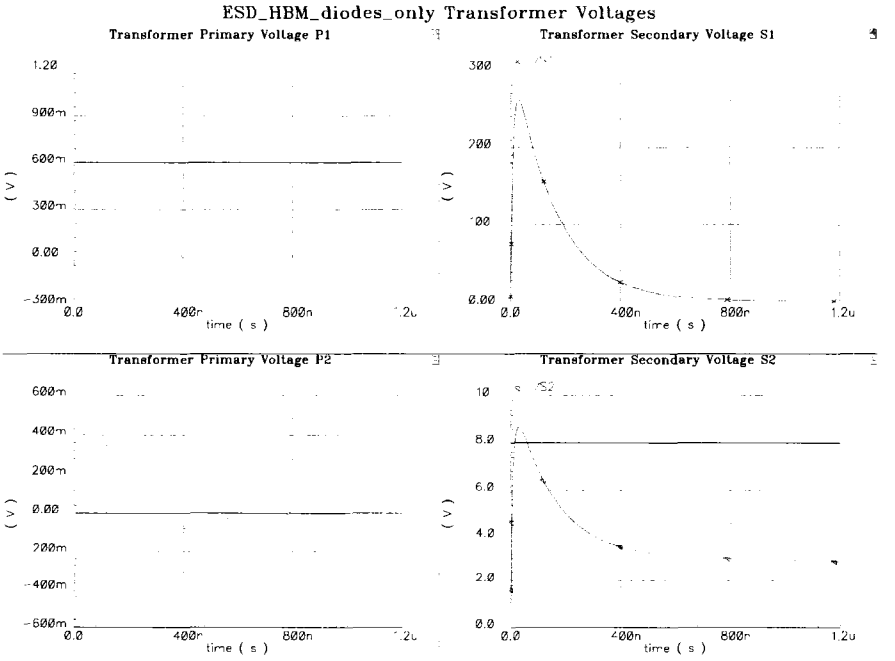

Figure 7.9 HBM without spark gaps: Transformer voltages

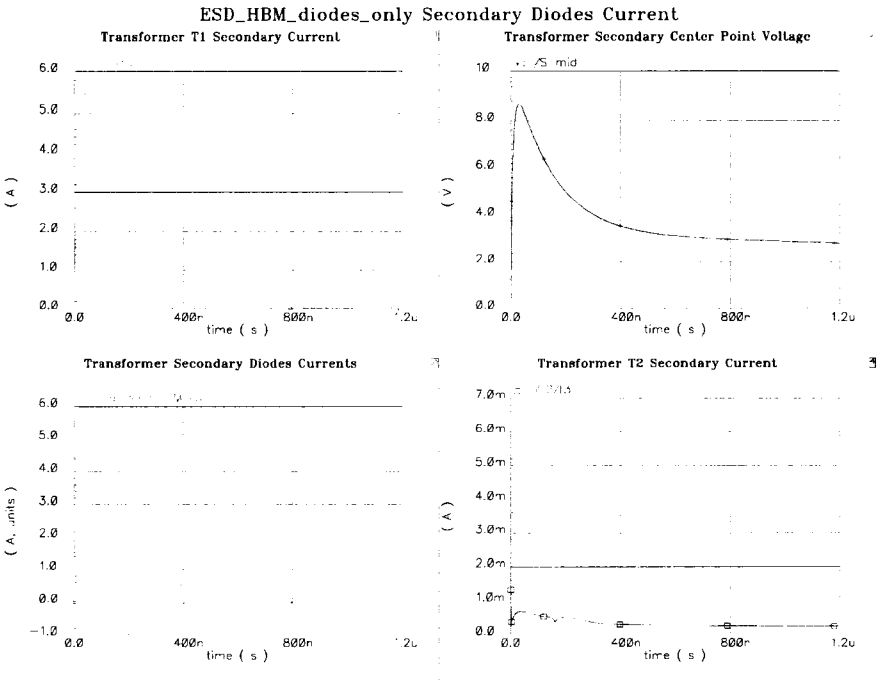

Figure 7.10 HBM without spark gaps: Transformer secondary currents

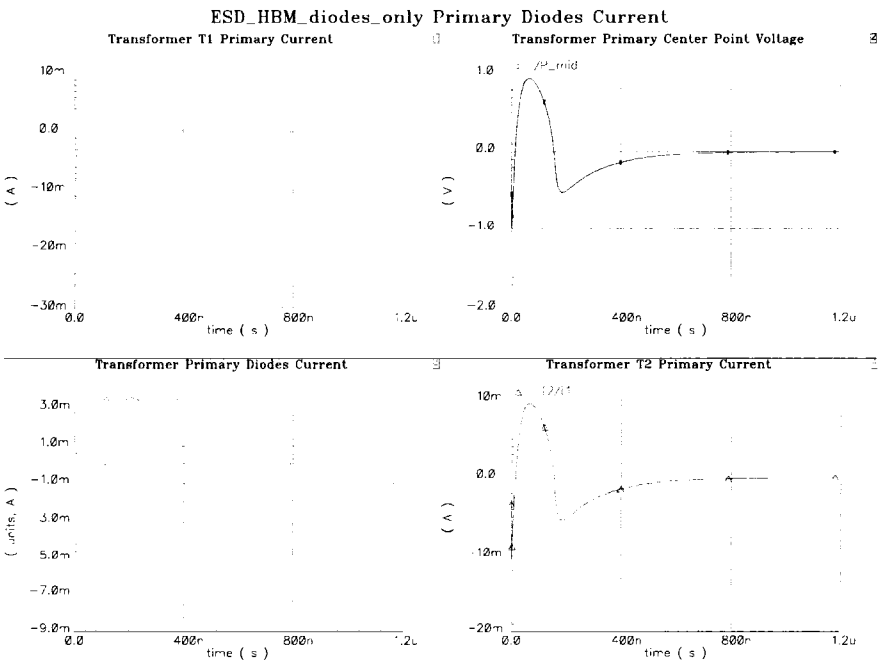

Figure 7.11 HBM without spark gaps: Transformer primary currents

7.9.2 HBM test for an ESD structure with spark gaps

The HBM simulation setup network consists of a 100 pF capacitor, a 15 uH inductor, a spark gap at each transformer secondary port, and a 1500Ω resistor. This test is applied to one of the input pads of the transformer secondary. The other input pad of the transformer secondary is left open as in Figure 7.12. A 50 termination resistor is placed at each transformer primary port.

The ESD voltage *Vs1*is displayed in Figure 7.13*L*. Figure 7.13*R*, shows the ESD current resulting from the discharge of the ESD capacitor. The current and voltage show a damped response due to the large ESD resistance 1500 Ω.

The transformer differential secondary voltage, $V_{secondary\_diff} = V_{S1} - V_{S2}$, Figure 7.14*UL*, raises in a damped response to around 3 V. The transformer differential primary voltage, $V_{primary\_diff} = V_{P1} - V_{P2}$, Figure 7.14*UR*, shows peaks at 80 mV and −10 mV. This voltage is well below the breakdown voltage, 2×4 V, of the NMOS differential pair transistors drains connected to it. This shows that the ESD structure provides protection to the internal circuit against voltages, at least, up to 10 kV. The frequency spectrum of $V_{secondary\_diff}$, $V_{secondary\_dft}$ in Figure 7.14*LL*, shows that the frequency components decrease rapidly after 500 MHz. The frequency spectrum of $V_{primary\_diff}$, ($V_{primary\_dft}$) shows attenuation in its magnitude as in Figure 7.14 *LR*.

Figure 7.15*UL*& *UR* shows the transformer secondary voltages V_{S1}, and V_{S2}, respectively. The response is damped, and settles down after 800 ns. The transformer primary voltages V_{P1}, and V_{P2} are displayed in Figure 7.15 *UL*, & *LL*, respectively. V_{P1} shows a maximum magnitude of 90 mV, while V_{P2} shows a maximum magnitude of 50 mV. The voltage transient lies comfortably below the 4V limit for each NMOS transistor connected to each port of the transformer primary.

Figure 7.16 displays the current waveforms of the transformer secondary. Figure 7.16*UL* is the ESD current that enters the secondary. The peak current is 33 mA. S_{mid} in Figure 7.16*UR* is the transformer secondary center point voltage. It rises to 1.5 V. Because $S_{mid} < V_{dd} + V_{t_{diode}}$, the top secondary diode in Figure 7.16*LL* continues to be in the OFF state. The situation

is the same for the secondary bottom diode which becomes biased and conducts most of the ESD current. The bottom secondary current is off as in Figure 7.16*LL*. There is a transient current in the primary top and bottom diodes due to charging and discharging the parasitic capacitances associated with the diode junctions. Almost all of the ESD current flows through the transformer T2 secondary windings as shown in Figure 7.16*LR*.

Figure 7.17 shows the current waveforms of the transformer primary. P_{mid} in Figure 7.17*UR* is the transformer secondary center point voltage. Figure 7.17*UL* is the ESD current that enters the primary. The negative current means that it is leaving the primary. The peak current is -1.7 mA. P_{mid} in Figure 7.17*UR* is the transformer primary center point. It rises to only 120 mV which is not enough to forward bias any of the primary diodes. There is a transient current, around 2 mA in the primary top and bottom diodes due to charging and discharging the parasitic capacitances associated with the diode junctions as shown in Figure 7.17*LL*. The rest of the current flows through the transformer T2 windings as shown in Figure 7.17*LR*.

As a conclusion, the ESD structure was able to protect the circuit against an HBM ESD event up to 10 kV. It should be noted that simulation shows that there is enough room to protect the circuit up to a higher voltage.

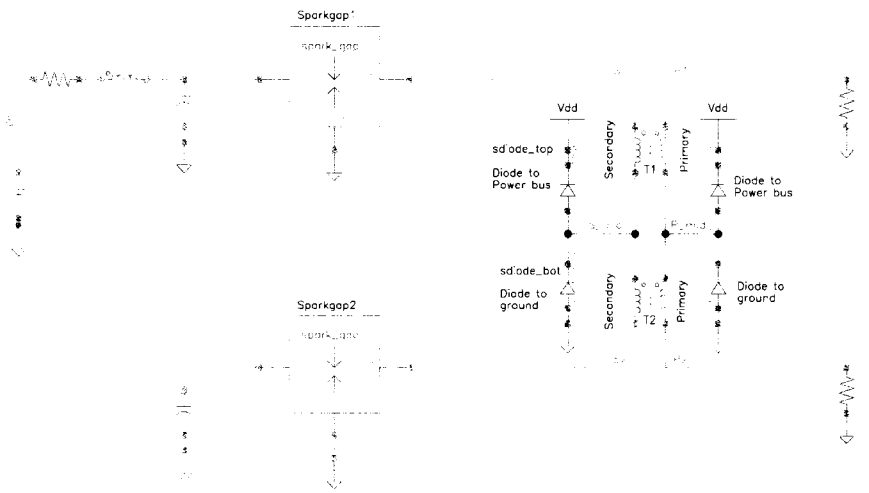

Figure 7.12 HBM with spark gaps: Schematic

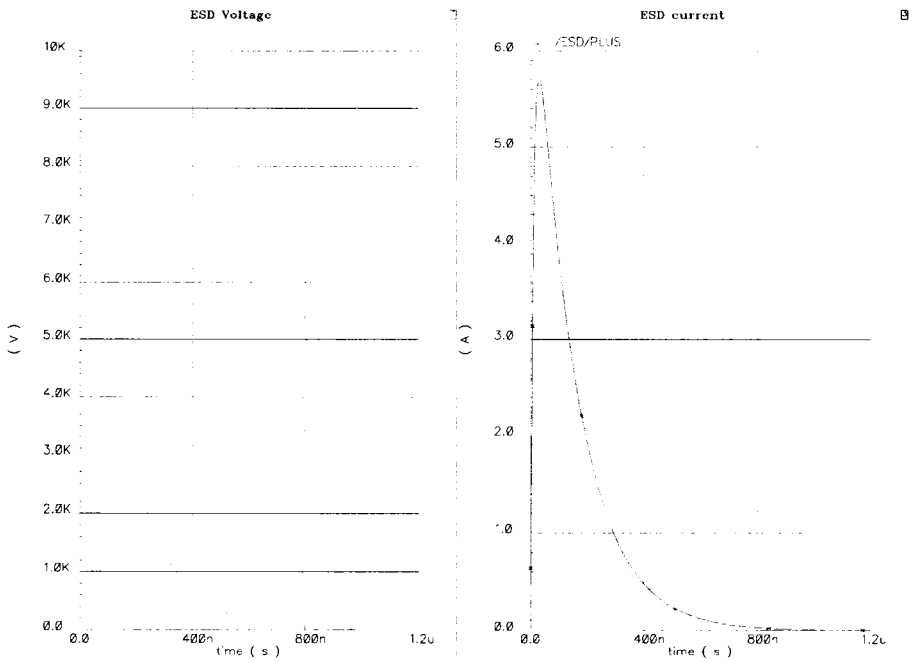

Figure 7.13 HBM with spark gaps: ESD current and voltage

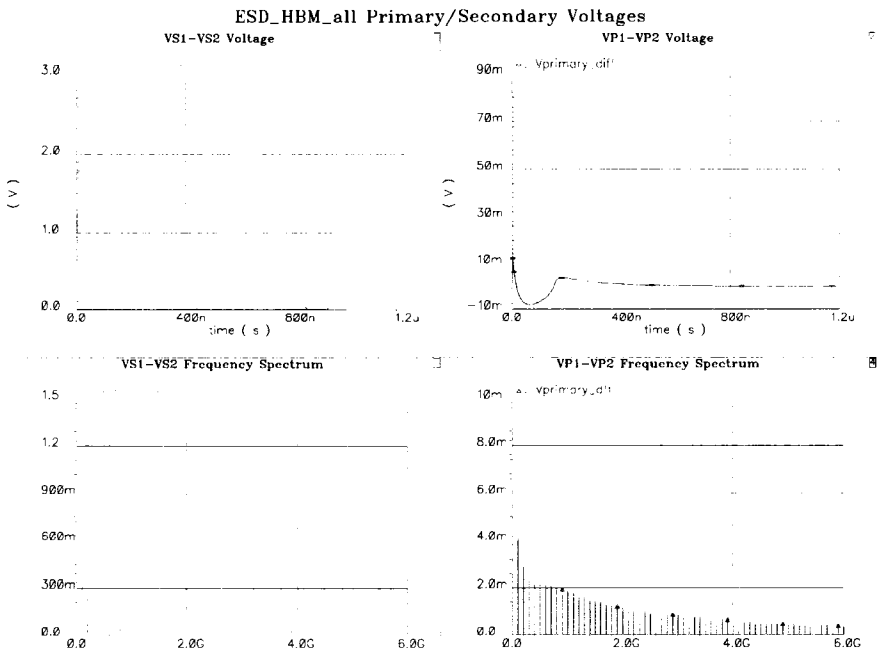

Figure 7.14 HBM with spark gaps: Sec. and pri. voltages

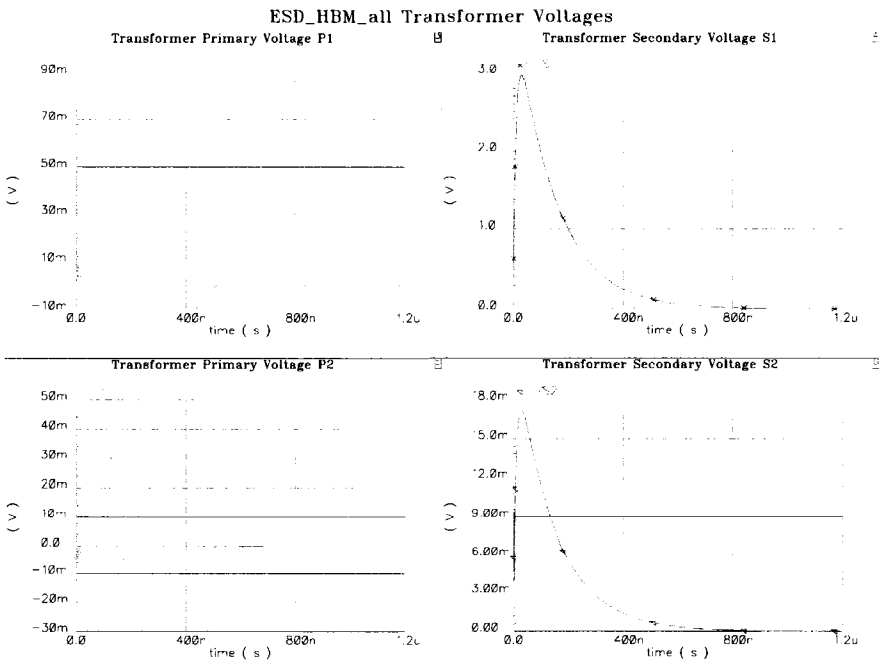

Figure 7.15 HBM with spark gaps: Transformer voltages

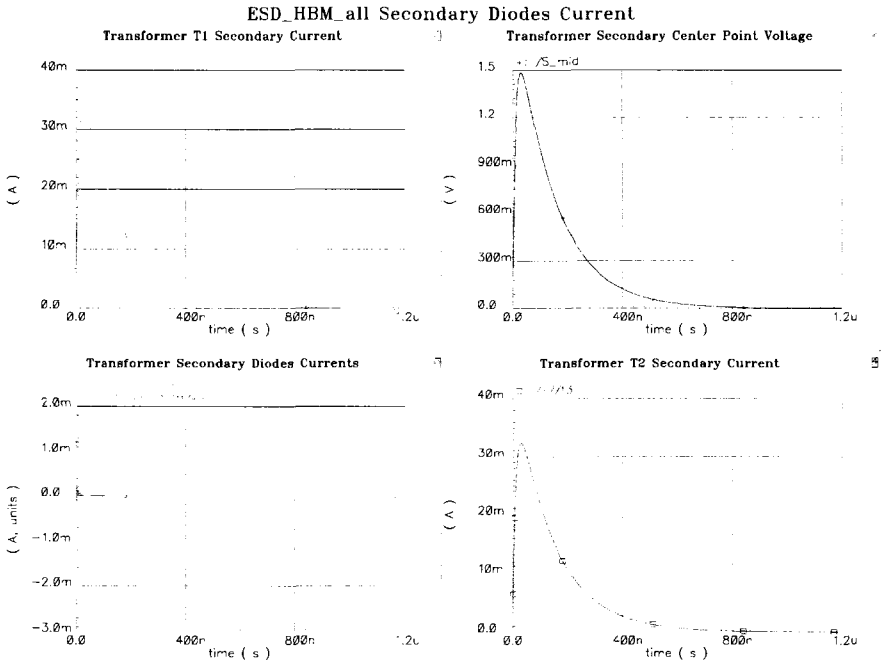

Figure 7.16 HBM with spark gaps: Transformer secondary currents

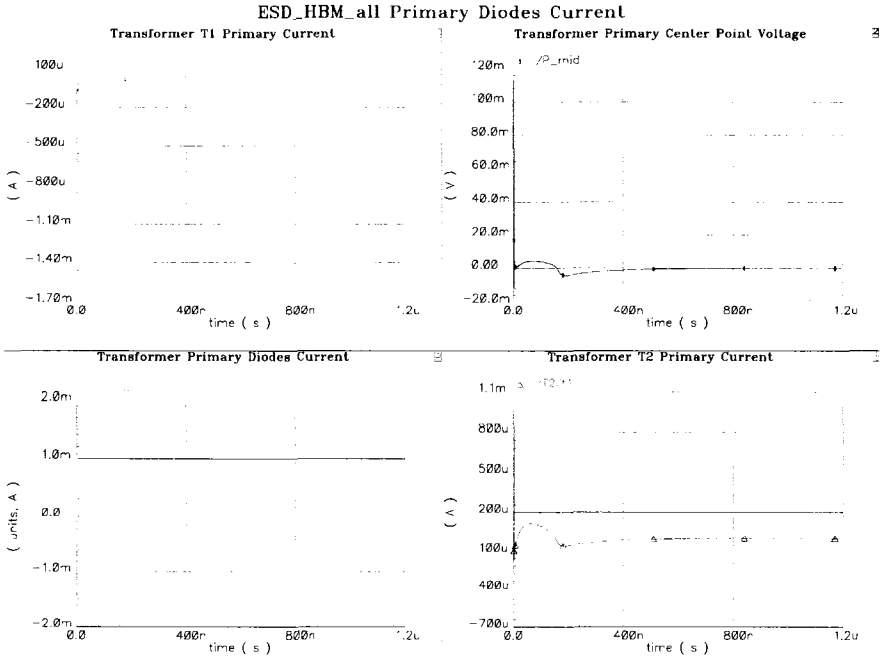

Figure 7.17 HBM with spark gaps: Transformer primary currents

7.10 Charged Device Model (CDM) test

7.10.1 CDM test for an ESD structure without spark gaps

The CDM simulation setup network consists of a 6.8 pF capacitor, a 100 nH inductor, and a 1Ω resistor. This test is applied to one of the input pads of the transformer secondary. The other input pad of the transformer secondary is left open as in Figure 7.18. A 50 termination resistor is placed at each transformer primary port. The ESD structure does not have the spark gaps included.

The ESD voltage V_{s1}, is displayed in Figure 7.19*L*. Figure 7.19*R* is the ESD current resulting from the discharge of the ESD capacitor. The current and voltage show an underdamped response due to the small ESD resistance 1Ω. It peaks at 1.5 A, and −0.7 A.

The transformer differential secondary voltage, $V_{secondary\_diff} = V_{S1} - V_{S2}$, Figure 7.20*UL*, (Figure 7.21*L*), rises in an underdamped response to 70 V. The transformer differential primary voltage, $V_{primary\_diff} = V_{P1} - V_{P2}$, Figure 7.20*UR*, (Figure 7.21*R*), shows peaks at 4.2 V and −2.5 V. This voltage is below the breakdown voltage, 2×4 V, of the combined NMOS transistors drains connected to it. This shows that the ESD structure provides protection to the internal circuit against voltages up to 250 V. The frequency spectrum of $V_{secondary\_diff}$, ($V_{secondary\_dft}$) in Figure 7.20 *LL*, shows that the frequency components are large in magnitude. This is a nature of the CDM ESD signal which has more frequency components at higher frequencies than the HBM case. It has less frequency components at lower frequencies. For example, it has a frequency component of around 1V at 1 GHz. The frequency spectrum of $V_{primary\_diff}$, $V_{primary\_dft}$ shows less attenuation in its magnitude as in Figure 7.20*LR*. It is noted that frequency components are shifted to a higher frequency band than in the HBM case. It has a frequency component of 150 mV at 1GHz. This is considerably higher than 25 mV in the HBM 10 kV case.

Figure 7.22 *UR*, & *LR*, (Figure 7.23*UR*, & *LR*) shows the transformer secondary voltages V_{S1}, andV_{S2}, respectively. The response is underdamped, and settles down after 15 ns. The change in voltage in V_{S2} is due to the turn on and off of the transformer secondary diodes.

The transformer primary voltages V_{P1}, andV_{P2} are displayed in Figure 7.22*UL*, & *LL*, (Figure 7.23*UL*, & *LL*) respectively. V_{P1} shows maximum magnitude of 3.9 V, while V_{P2} shows a maximum magnitude of 1.1 V. The voltage transient lies just below the 4V limit for each NMOS transistor connected to each port of the transformer primary.

Figure 7.24 displays the current waveforms of the transformer secondary. Figure 7.24*UL*, (Figure 7.25*UL*) is the ESD current that enters the secondary. The peak current is 1.5 A. S_{mid} in Figure 7.24*UR*, (Figure 7.25*UR*) is the transformer secondary center point voltage. It rises to 3.2 V. Because $S_{mid} > Vdd + V_{t_{diode}}$, the top secondary diode in Figure 7.25*LL*is forward biased and conducts most of the ESD current. The bottom secondary current is off as in Figure 7.25*LL*. When S_{mid} drops to -2 V at $t = 4$ ns, the top secondary diode in Figure 7.25*LL*is reverse biased and conducts no ESD current. The bottom secondary current is on and conducts most of the current as in Figure 7.25*LL*untill $t = 6$ ns. Another indication that most of the ESD current is dissipated in the diodes is the transformer T2 secondary current in Figure 7.25*LR*. The magnitude of the current peak is less than 15 mA. This is about 1% of the original ESD current.

Figure 7.26 shows the current waveforms of the transformer primary. Figure 7.26*UL*, (Figure 7.27*UL*) is the ESD current that enters the primary. The negative current means that it is leaving the primary. The peak current is -75 mA. P_{mid} in Figure 7.26*UR*(Figure 7.27*UR*) is the transformer primary center point. It rises to only 2 V which is not enough to forward bias the top primary diodes. There is a transient current in the primary top and bottom diodes due to charging and discharging the parasitic capacitances associated with the diodes junctions as shown in Figure 7.26*LL*, (Figure 7.27*LL*). Most of the current flows through the transformer T2 windings as shown in Figure 7.26*LR*, (Figure 7.27*LR*).

As a conclusion, the ESD structure was able to protect the circuit against an CDM ESD event up to only 250 V. In many cases, this amount of protection is not adequate for typical ESD events. Deployment of spark gaps is necessary to improve the ESD protection level.

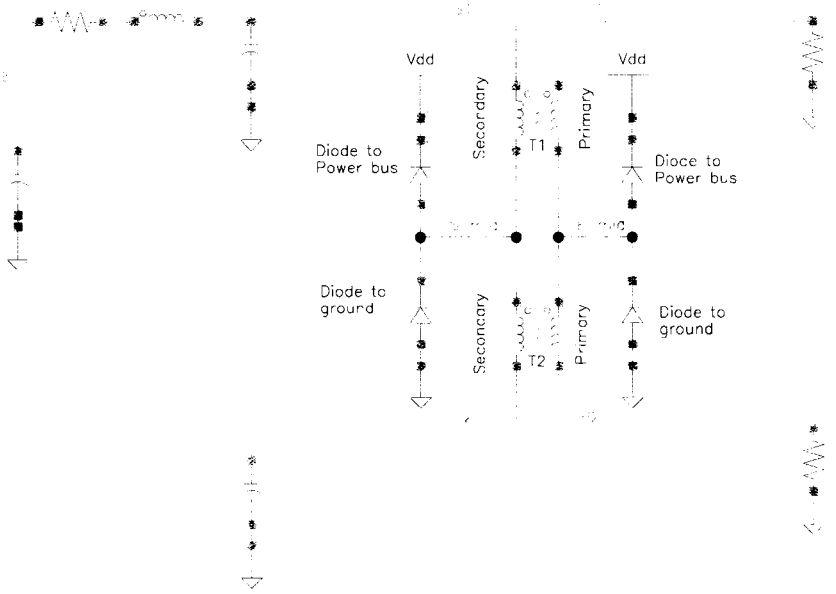

Figure 7.18 CDM without spark gaps: Schematic

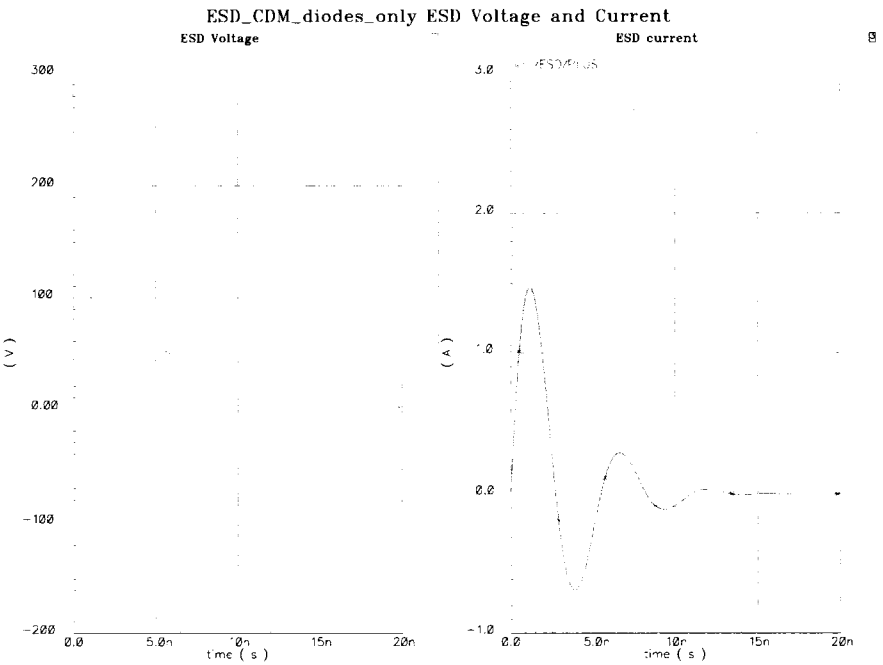

Figure 7.19 CDM without spark gaps: ESD current and voltage

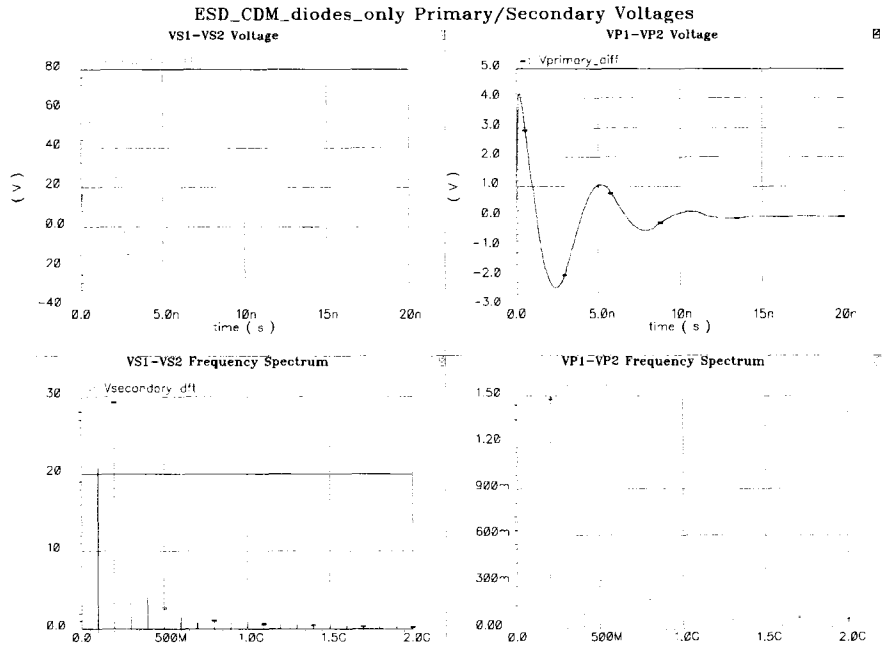

Figure 7.20 CDM without spark gaps: Sec. and pri. voltages

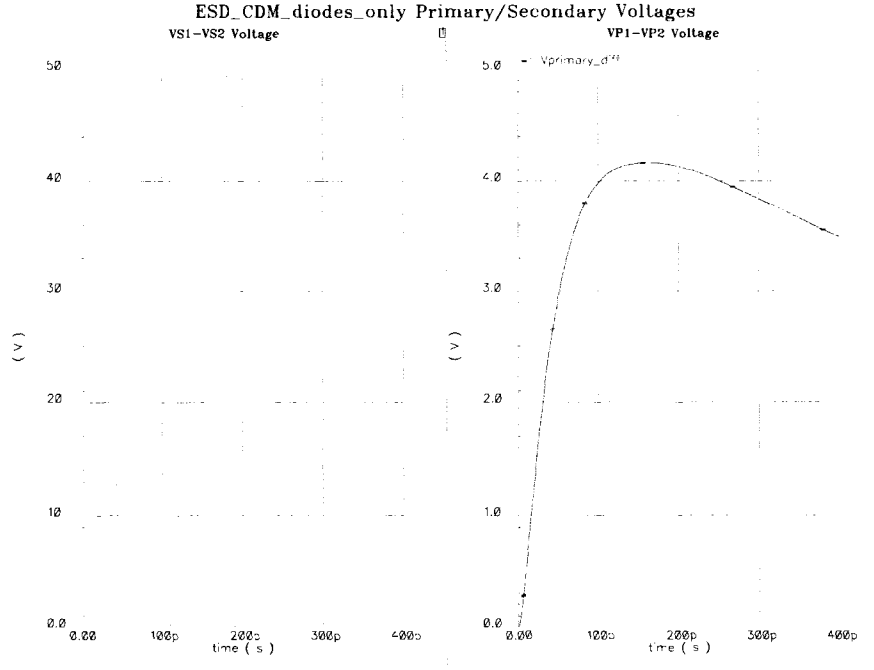

Figure 7.21 CDM without spark gaps: Sec. and pri. voltages *(zoom)*

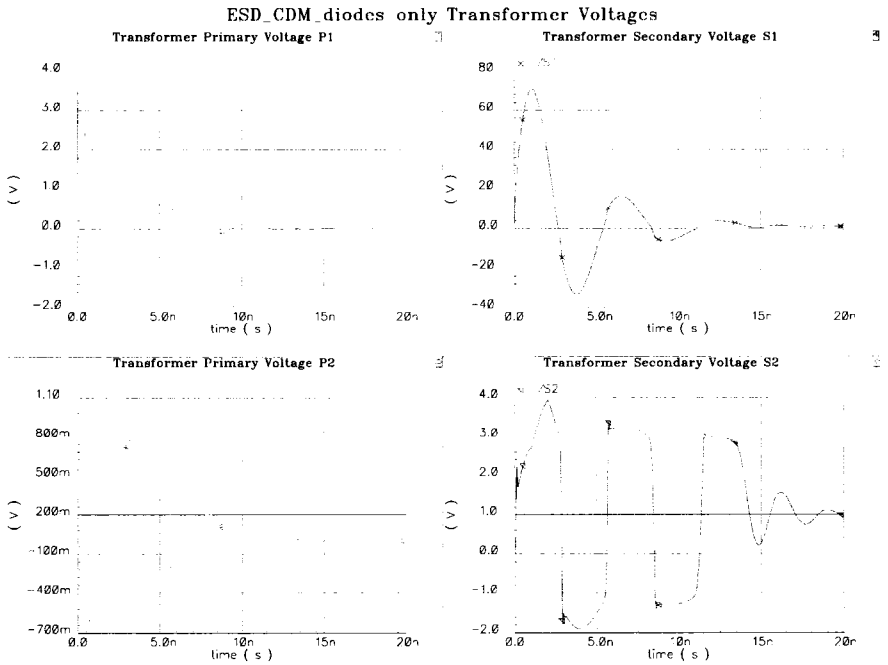

Figure 7.22 CDM without spark gaps: Transformer voltages

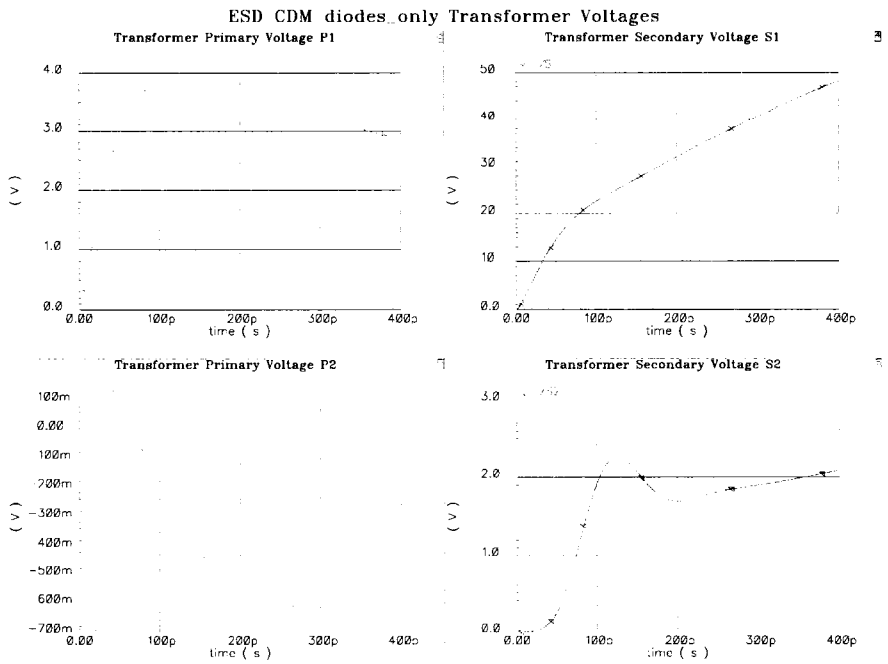

Figure 7.23 CDM without spark gaps: Transformer voltages *(zoom)*

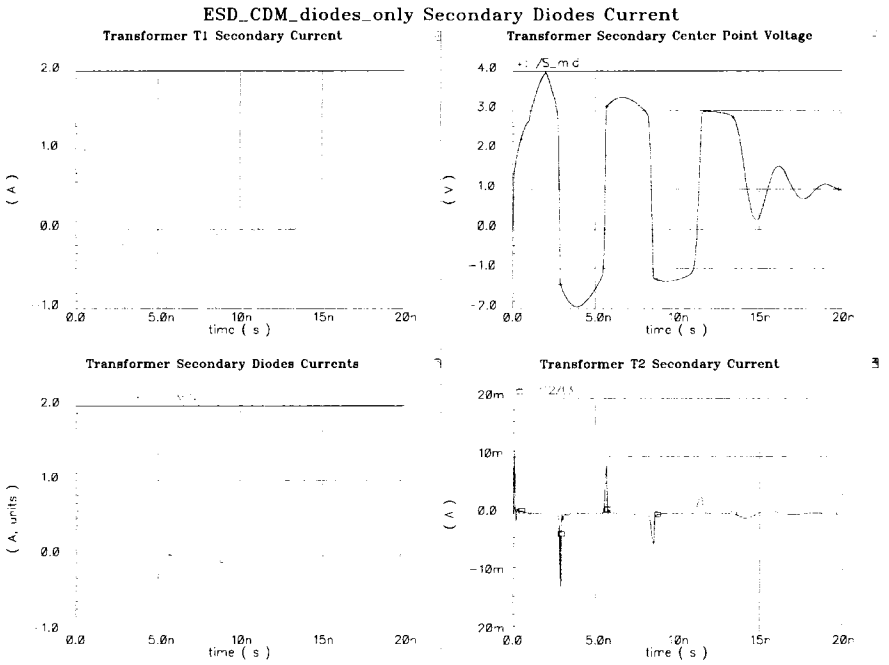

Figure 7.24 CDM without spark gaps: Transformer secondary currents

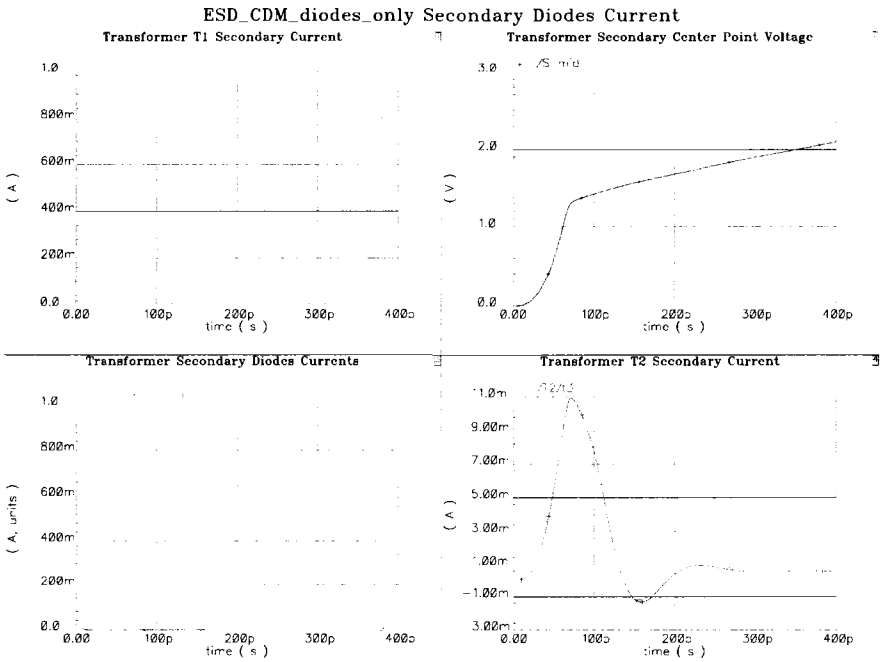

Figure 7.25 CDM without spark gaps: Transformer secondary currents *(zoom)*

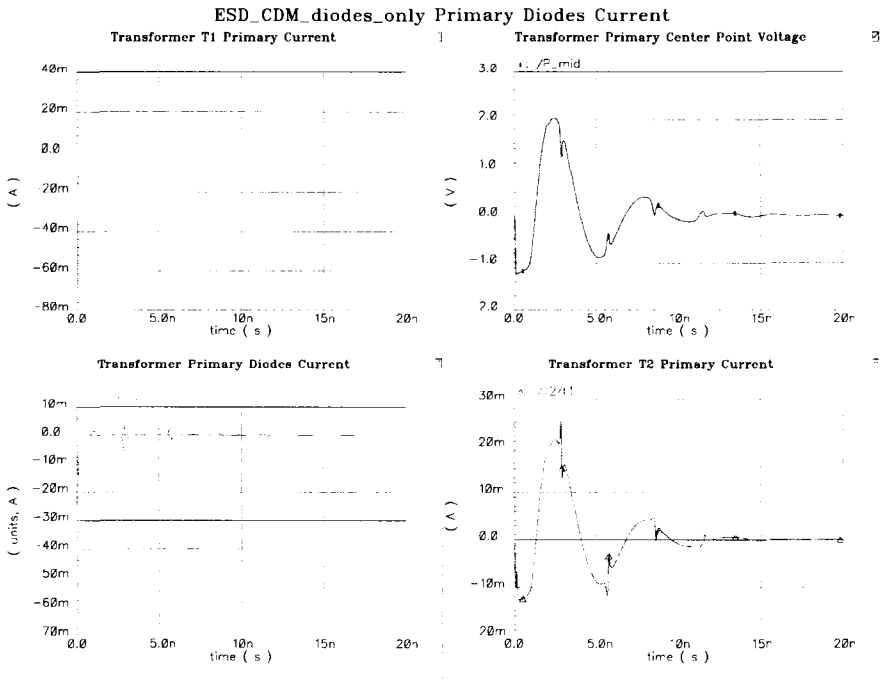

Figure 7.26 CDM without spark gaps: Transformer primary currents

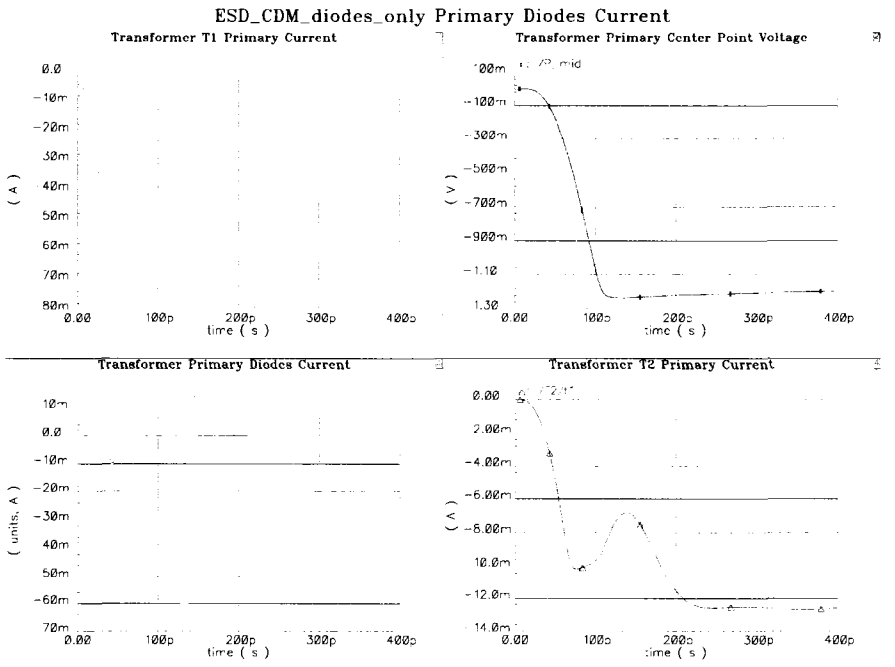

Figure 7.27 CDM without spark gaps: Transformer primary currents *(zoom)*

7.10.2 CDM test for an ESD structure with spark gaps

The CDM simulation setup network consists of a 6.8 pF capacitor, a 100 nH inductor, a spark gap at each transformer secondary port, and a 1Ω resistor. This test is applied to one of the input pads to the transformer secondary. The other input pad of the transformer secondary is left open as in Figure 7.28. A 50 termination resistor is placed at each transformer primary port.

The ESD voltage *Vs1*is displayed in Figure 7.29,*L*. Figure 7.29*R*, shows the ESD current resulting from the discharge of the ESD capacitor. The current and voltage show an underdamped response due to the small ESD resistance 1 Ω. It peaks at 24 A, and −21 A.

The transformer differential secondary voltage, $V_{secondary\_diff} = V_{S1} - V_{S2}$, Figure 7.30*UL*,(Figure 7.31*L*), rises in an underdamped response to 19 V. The transformer differential primary voltage, $V_{primary\_diff} = V_{P1} - V_{P2}$, Figure 7.30*UR*, (Figure 7.31*R*), peak at 4.0 V and −0.9 V. This voltage is below the breakdown voltage, 2 × 4 V, of the combined NMOS transistors drains connected to it. This shows that the ESD structure provides protection to the internal circuit against voltages up to 3*k* V. The frequency spectrum of $V_{secondary\_diff}$, $V_{secondary\_dft}$ in Figure 7.30*LL*, shows that the frequency components are large in magnitude. This is a nature of the CDM ESD signal which has comparable frequency components to the CDM case without spark gaps. For example, it has a frequency component of around 1V at 1 GHz. The frequency spectrum of $V_{primary\_diff}$, $V_{primary\_dft}$ shows a peak of 0.8 V in its magnitude as in Figure 7.30*LR*. It has a frequency component of 150 mV at 1 GHz. This is close to the 150 mV in the CDM 250 V case.

Figure 7.32 *UR*& *LR*, (Figure 7.33*UR*& *LR*) show the transformer secondary voltages $V_{S1}, \text{and} V_{S2}$, respectively. The response is underdamped, and settles down after 40 ns. The change in voltage in V_{S2} is due to the turn on and off of the transformer secondary diodes. The transformer primary voltages $V_{P1}, \text{and} V_{P2}$ are displayed in Figure 7.32*UL*& *LL*, (Figure 7.33*UL*& *LL*) respectively. V_{P1} shows a maximum magnitude of 3.9 V, while V_{P2} shows a maximum magnitude of 0.7 V. The voltage transient lies just below the 4V limit for each NMOS transistor connected to each port of the transformer primary.

Figure 7.34 displays the current waveforms of the transformer secondary. Figure 7.34*UL*, (Figure 7.35*UL*) gives the ESD current that enters the secondary. The peak current is 0.35 A. S_{mid} in Figure 7.34*UR*, (Figure 7.35*UR*) is the transformer secondary center point voltage. It rises to 3.2 V. Because $S_{mid} > V_{dd} + V_{t_{diode}}$, the top secondary diode in Figure 7.34*LL*is forward biased and conducts most of the ESD current. The bottom secondary current is off as in Figure 7.34*LL*. When S_{mid} drops to -1.6 V at $t = 2, 7.5$ ns, the top secondary diode in Figure 7.34*LL*is reverse biased and conducts no ESD current. The bottom secondary current is on and conducts most of the current as in Figure 7.34*LL*till $t = 4.5, 10$ ns. Another indication that a considerable part of the ESD current is dissipated in the diodes is the transformer T2 secondary current in Figure 7.34*LR*, (Figure 7.35*LR*). The magnitude of the current peak is less than 70 mA. This is about 20% of the original ESD current. The rest is dissipated in the diodes.

Figure 7.36 shows the current waveforms of the transformer primary. Figure 7.36*UL*, (Figure 7.37*UL*) is the ESD current that enters the primary. The negative current means that it is leaving the primary. The peak current is -75 mA. P_{mid} in Figure 7.36*UR*, (Figure 7.37*UR*) is the transformer primary center point. It rises to less than 1 V which is not enough to forward bias the top primary diodes. There is a transient current in the primary top and bottom diodes due to charging and discharging the parasitic capacitances associated with the diodes junctions as shown in Figure 7.36*LL*(Figure 7.37*LL*). Most of the current flows through the transformer T2 windings as shown in Figure 7.36*LR*, (Figure 7.37*LR*).

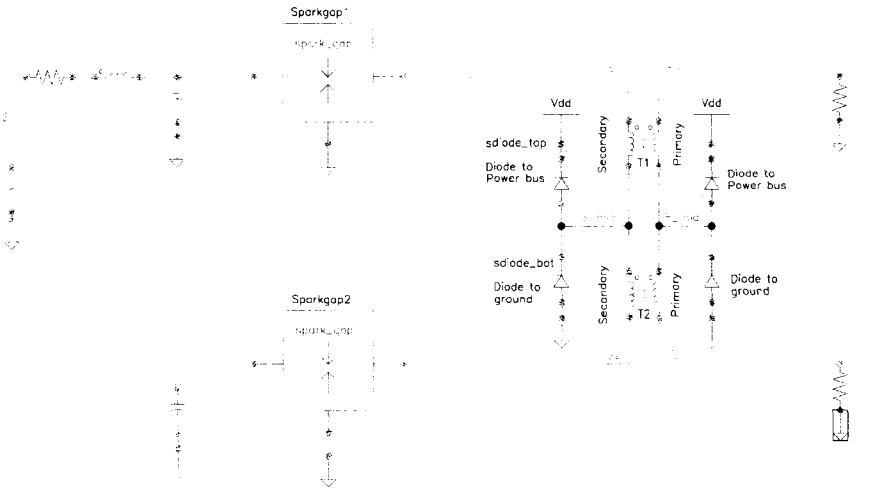

Figure 7.28 CDM with spark gaps: Schematic

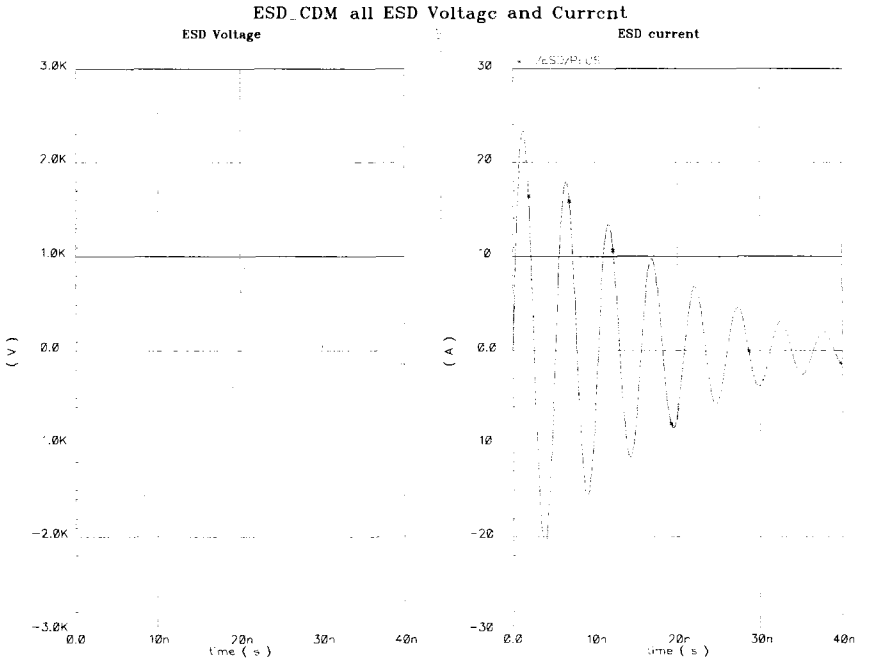

Figure 7.29 CDM with spark gaps: ESD current and voltage

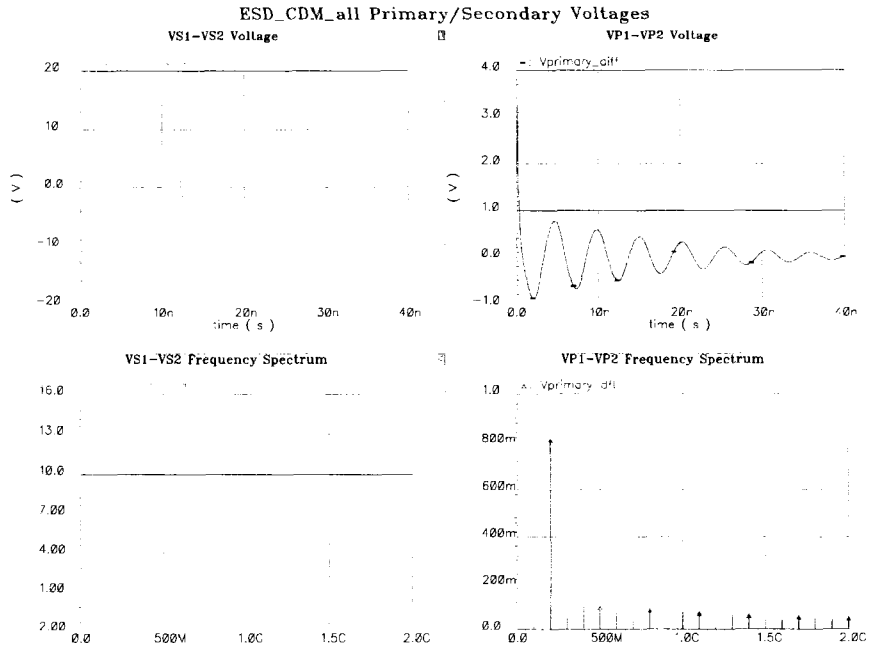

Figure 7.30 CDM with spark gaps: Sec. and pri. voltages

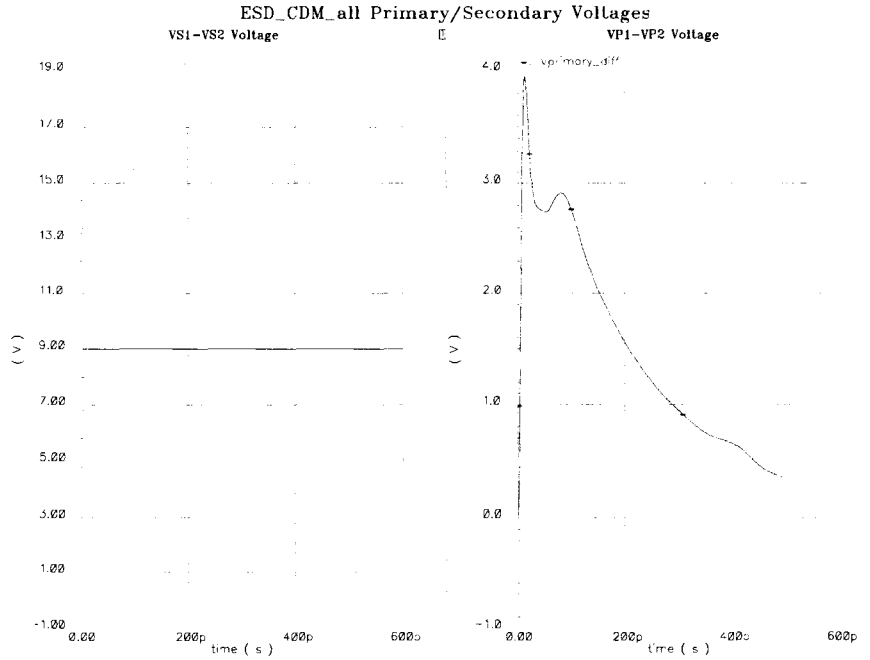

Figure 7.31 CDM with spark gaps: Sec. and pri. voltages *(zoom)*

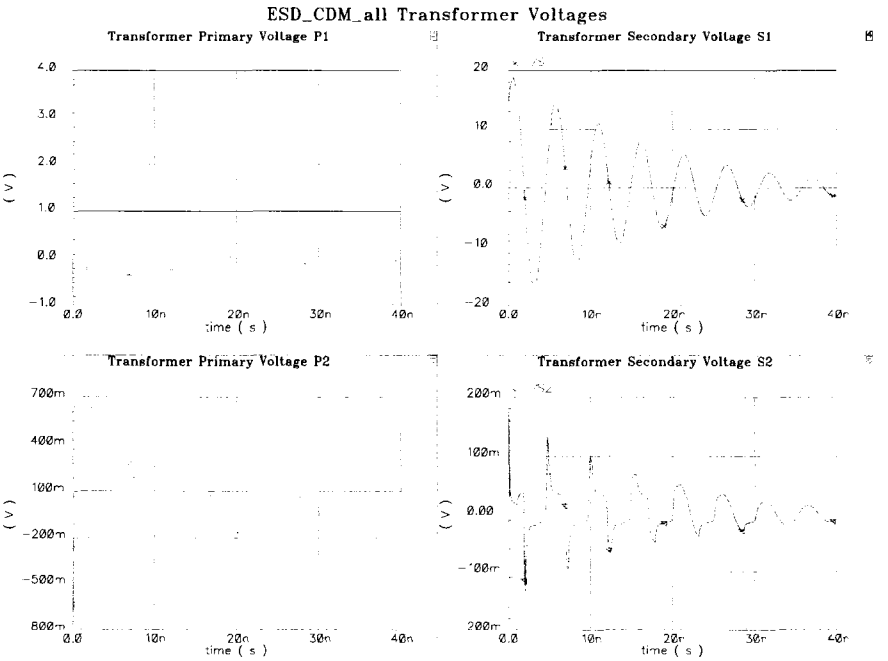

Figure 7.32 CDM with spark gaps: Transformer voltages

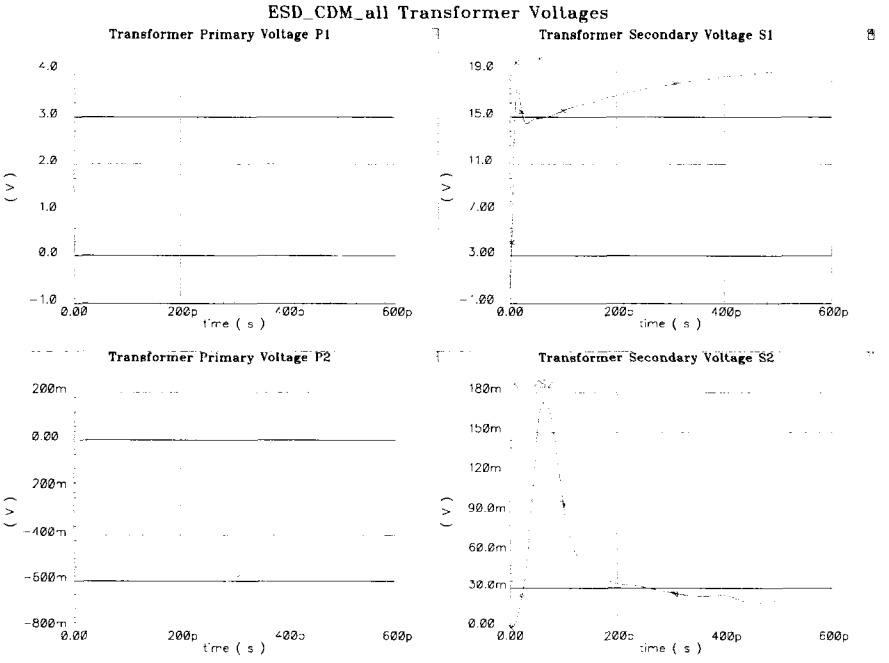

Figure 7.33 CDM with spark gaps: Transformer voltages *(zoom)*

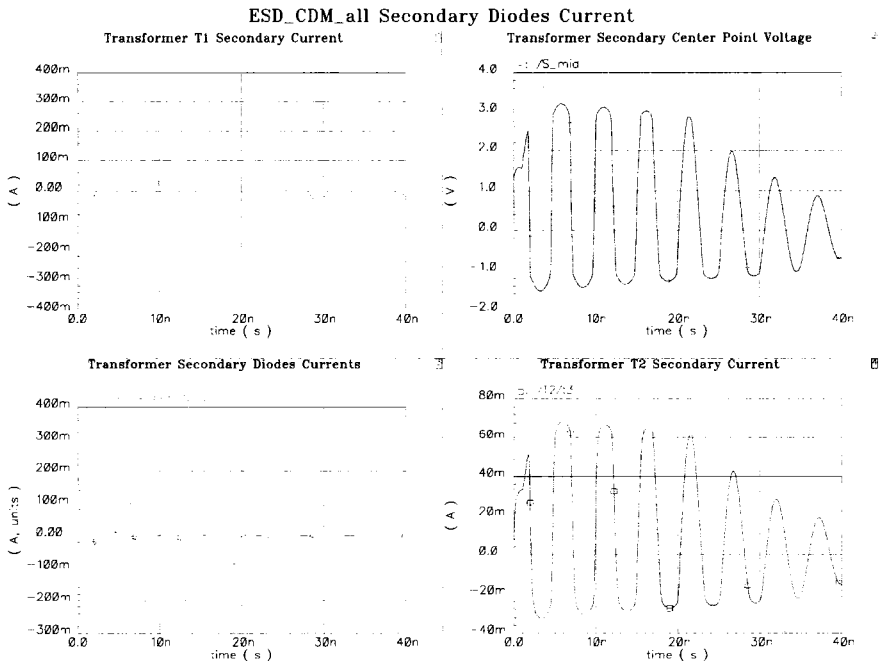

Figure 7.34 CDM with spark gaps: Transformer secondary currents

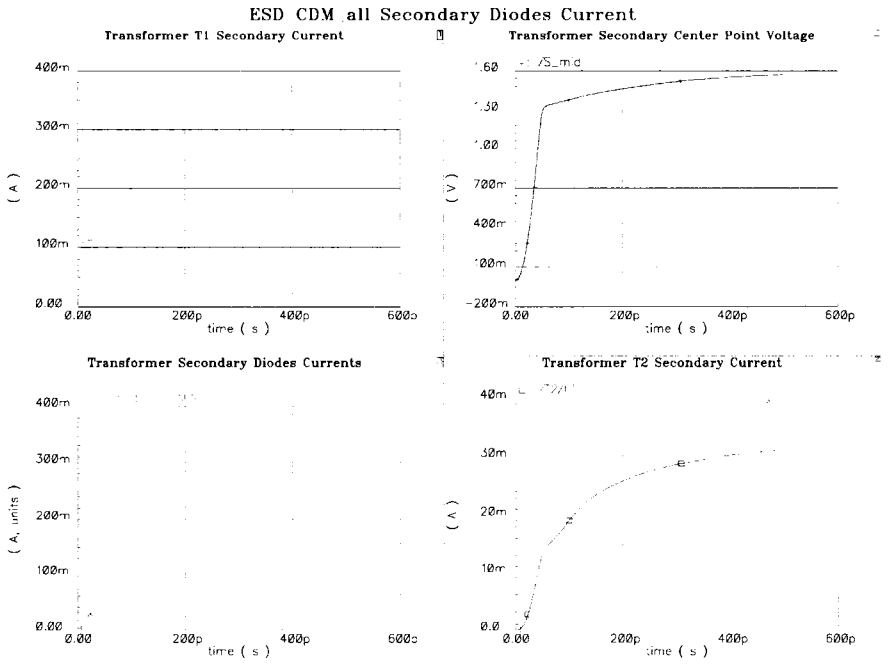

Figure 7.35 CDM with spark gaps: Transformer secondary currents *(zoom)*

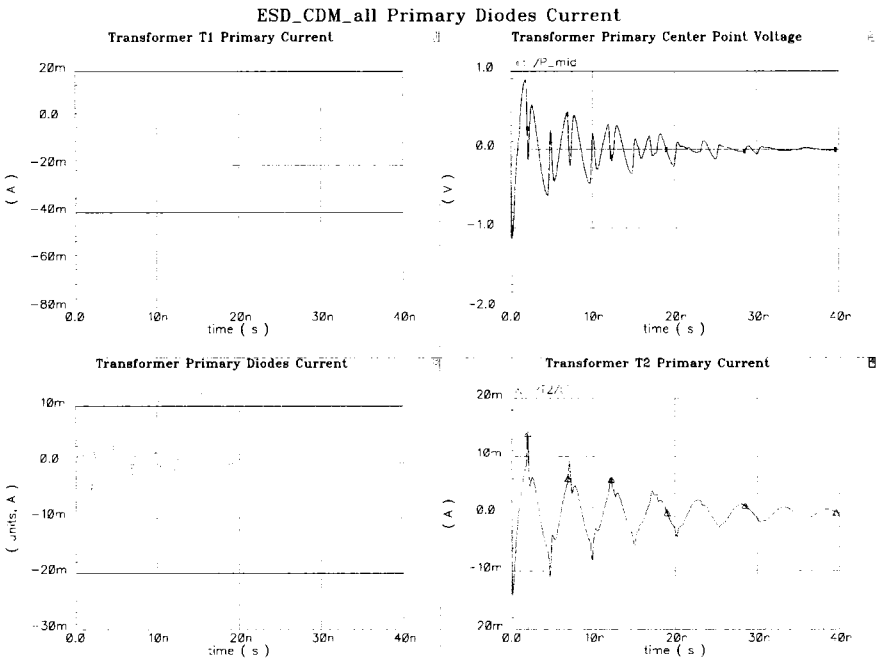

Figure 7.36 CDM with spark gaps: Transformer primary currents

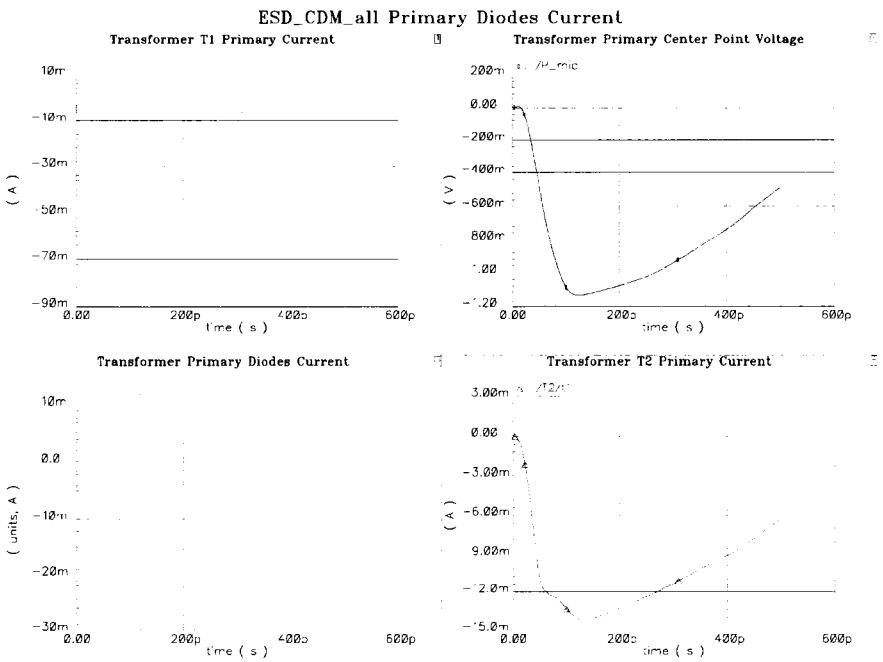

Figure 7.37 CDM with spark gaps: Transformer primary currents *(zoom)*

7.11 Contribution summary

The contribution represented by this chapter is a design of an RF and Gbit/s ESD structure using monolithic transformers and on-chip spark gaps. The design shows a protection level up to 10 kV for the HBM case, and 3 kV in the CDM case. The bandwidth of the device is from 1.5-6 GHz. A comparison of the results of the proposed ESD structure to existing state of the art RF ESD protection methods is presented in Table 7.1. The proposed methods prove, through simulations, to be competitive to other ESD protection methods.

Table 7.1 ESD Protection Methods: Comparison of results

Protection Method	C_{tot} (fF) (No pads)	HBM (Volts)	CDM (Volts)
NO ESD	0	4	4
Low Speed Methods	$\sim$ 1000	2k-4k	2k-4k
[53]	150	2k	N/A
[25]	90	4k	N/A
Proposed(w/o spark gaps)	44	10k	250
Proposed(w spark gaps)	46	10k	3k

CHAPTER 8. Driver design and encoding schemes

8.1 Introduction

In this chapter two driver-encoding schemes are discussed. The first one is a DC balancing scheme to guarantee that the average signal on the line at any point in time is substantially zero. In this way, the DC value of the signal on the line is stabilized. The second encoding scheme focuses the energy content of the signal around one frequency so that the driver can be terminated easily with termination resistors.

8.2 DC balancing encoding

This encoding scheme gives the signaling scheme several features:

1. It provides DC balancing of the signal on the line.

2. It provides easier clock recovery for the signal at the receiver. Therefore no clock signal needs to be sent to the receiver on a separate line. This will give maximum efficiency of the pin number utilization.

3. It provides error detection of the transmitted signal at the receiver. This is because after every predetermined number of bits is sent, the average of the signal on the line is zero.

Figure 8.1 illustrates the encoder block diagram. As an example, the data enters a 5 to 1 multiplexer over 4 buses according to 5 phases of the clock. The fifth bus is a control signal. There's no fifth data bus. According to the clock, the multiplexer chooses, according to the clock phase, one of the buses one at a time. The chosen data bus M1-M0 then enters the thermometer encoder. At f4, there is no data that enters the thermometer encoder. The table

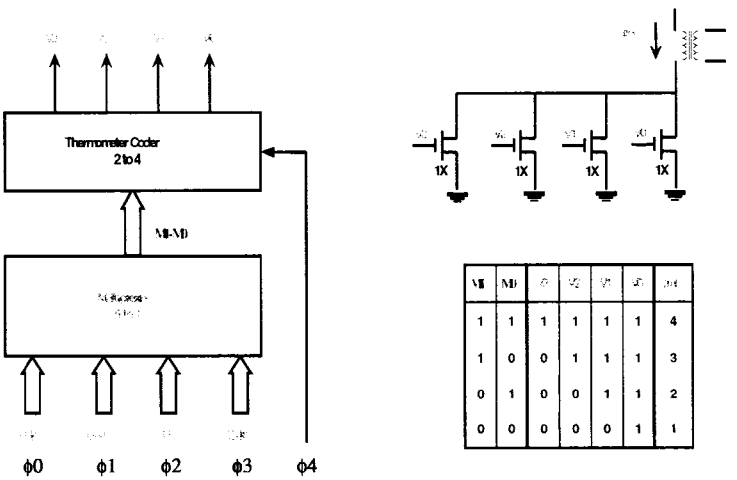

Figure 8.1 DC balancing encoder

in Figure 8.1 shows the relation between the input and output of the thermometer encoder. At no point in time is the output of the thermometer encoder completely zero in all of its outputs. The output of the thermometer encoder enters the driver. The voltage levels of the driver input are as follows. A high voltage is high enough to let the corresponding transistor enter its saturation region. A low voltage lets the transistor shut off. As can be seen, the driver acts as a voltage to a current converter. The output is a multilevel current signal that is sent to the transformer. The transformer then differentiates that current into an induced voltage at the secondary to be sent to the line. This is illustrated in Figure 8.1.

8.3 4to5 bus encoding

This encoding scheme takes place before the multiplexer. Each bit from each bus is encoded such that there is a maximum number of transitions from one bus word to another bus word. This logical block contributes to the termination scheme such that it's easier to use a simple termination resistor at the driver. This encoding scheme focuses the signal frequency content around a certain frequency.

Table 8.1 shows an analysis of the number of transitions in 4 bit words. As an example a 1111 or 0000 have 0 number of transitions.

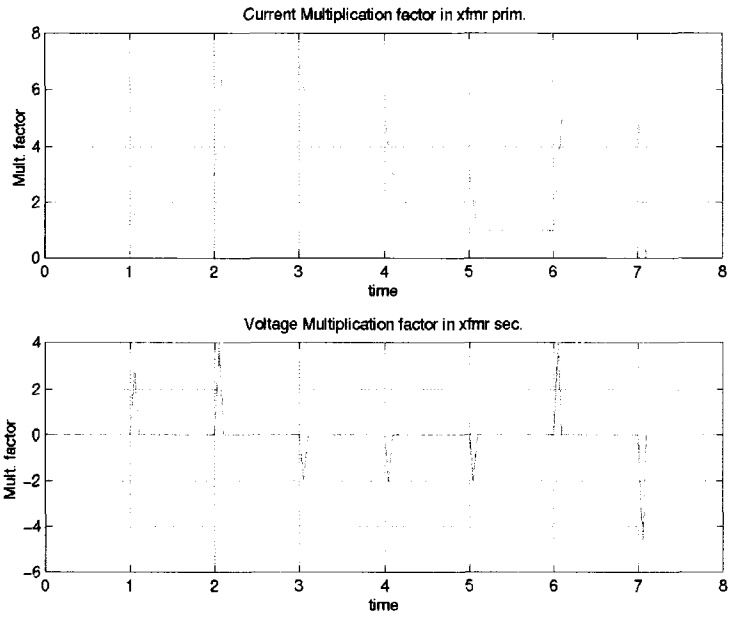

Figure 8.2 Waveforms at the transformer primary and secondary

Table 8.1 Analysis of transition in 4 bit words

no. of trans. Cases for 4 bit word	no. of trans. For 4 bit word before encoding
2	0
6	1
6	2
2	3

Table 8.2 shows the number of transitions is narrowed down from a wide spectrum of 0 to 3 transitions to 2 to 3 transitions. With the addition of the DC balancing code, the number of transitions is increased by 1. Equation 8.1 shows the encoding function used.

$$A_i = A_j \tag{8.1}$$

$$B_i = B_j \tag{8.2}$$

$$C_i = \overline{D_j}C_j + A_jC_j + \overline{A_jB_j}C_j + \overline{A_jB_j}D_j \tag{8.3}$$

$$D_i = C_jD_j + B_jD_j + A_jD_j + \overline{B_jC_jD_j} \tag{8.4}$$

$$E_i = \overline{C_j}D_j + A_jD_j\overline{B_j} + \overline{D_j}A_jB_j \tag{8.5}$$

Table 8.2 Analysis of transitions after adding one extra bit to word

no. of trans. Cases for 5 bit word	no. of trans. after encoding	Trans. with DC balance
12	2	3
4	3	4

(8.6)

8.4 Driver matching

The driver has to be matched, at the transformer, to the line. Since the transformer acts as a high pass filter, the transformer has to be matched to the line from the cutoff frequency (2GHz) to around 5 GHz. The matching problem can be solved using a lossless matching network composed of capacitors and inductors between the driver and the PCB line. Another method is to use a resistive matching network. The problem with it is the high loss that occurs at the driver.

8.5 Driver architecture

8.5.1 Current mode driver

In the Current Model Driver, the driver is directly connected to the bonding wire. The ESD devices are connected to the signal nodes at the drivers as in Figure 8.3. The benchmark used in this test is the maximum clock sent from the driver to the receiver. Simulation results in HSPICE, in 0.18u CMOS process, show that it can pass a maximum clock of 1.14 GHz. For a differential signal swing of 200 mV at the receiver, the maximum bit rate sent from the driver to the receiver is 2.28 Gbit/s as in Figure 8.4.

8.5.2 Transformers in driver structure

The driver is composed of a differential pair with the transformers connected to the drains of the differential pair. The loads can be plain resistors or transistors in the triode region as shown in Figure 8.5. The driver uses current mode signal to pass to the transformer. The

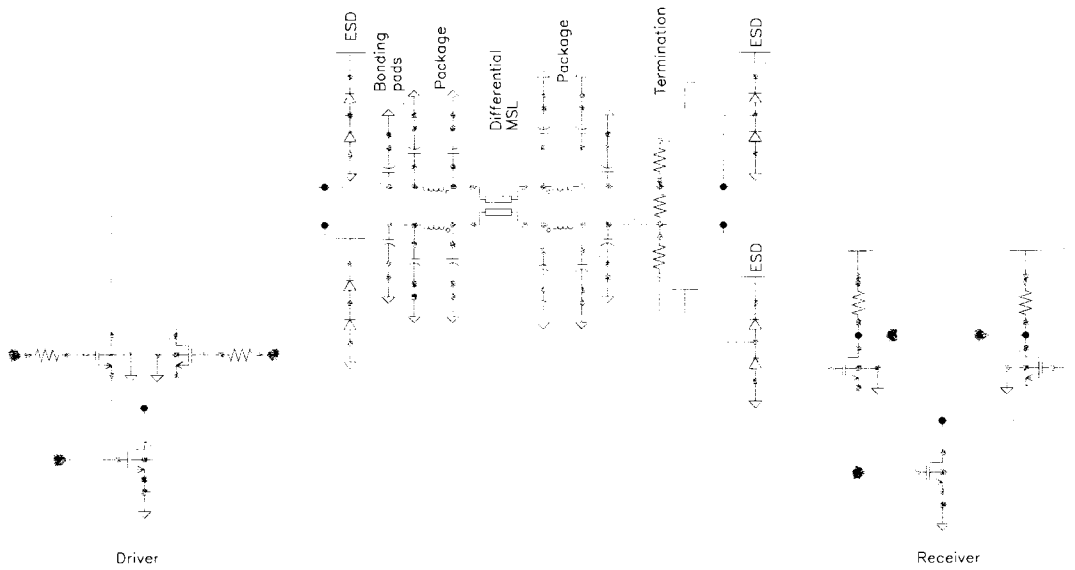

Figure 8.3 Current Mode Driver

driver rise time is controlled by the use of several transistors with their drains and sources connected together but the gates are connected in series through a set of resistors [14]. The transformer model is shown in Figure 8.6.

In Figure 8.7, the driver is shown in addition to the PCB MSL and receiver front end. The driver has rise time control. The receiver has a pair of transformers that work as ESD structures and as part of the receiver front end.

This structure has an advantage over the previous structure in that the current consumption is less. The reason is that in Figure 8.5 the current has to pass through the parallel combination of the termination resistors and the transformers pair. This happens when the differential pair switch current between its sides. On the other hand, the structure in 8.7 has the whole current in the driver transistors passing in the transformer, and not a part of it as in 8.5. It is noted that the differential pair transistors need not shut off completely when the current in transferred between its sides.

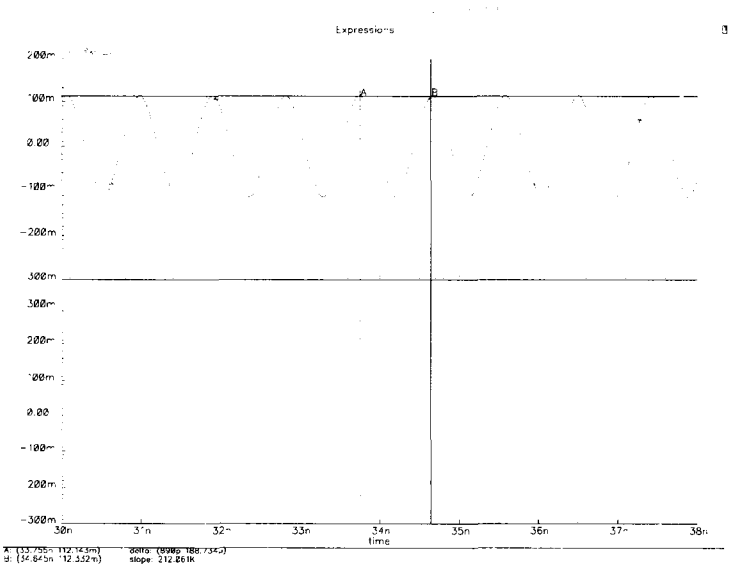

Figure 8.4 Current mode driver maximum bit rate

8.5.3 Transformer isolation scheme simulation

In the Transformer Isolation Scheme (TIS), the transformers are connected to the driver and at the receiver as in Figure 8.8. ESD devices are present in the driver an at the receiver. The length of the GML PCB trace is 5 inches. Simulation is made in HSPICE for 0.18u CMOS process. For a differential signal swing of 200 mV at the receiver, the maximum bit rate sent from the driver to the receiver is 10.6 Gbit/s as shown in Figure 8.9. The minimum bit rate is 3.8 Gbit/s as in Figure 8.10.

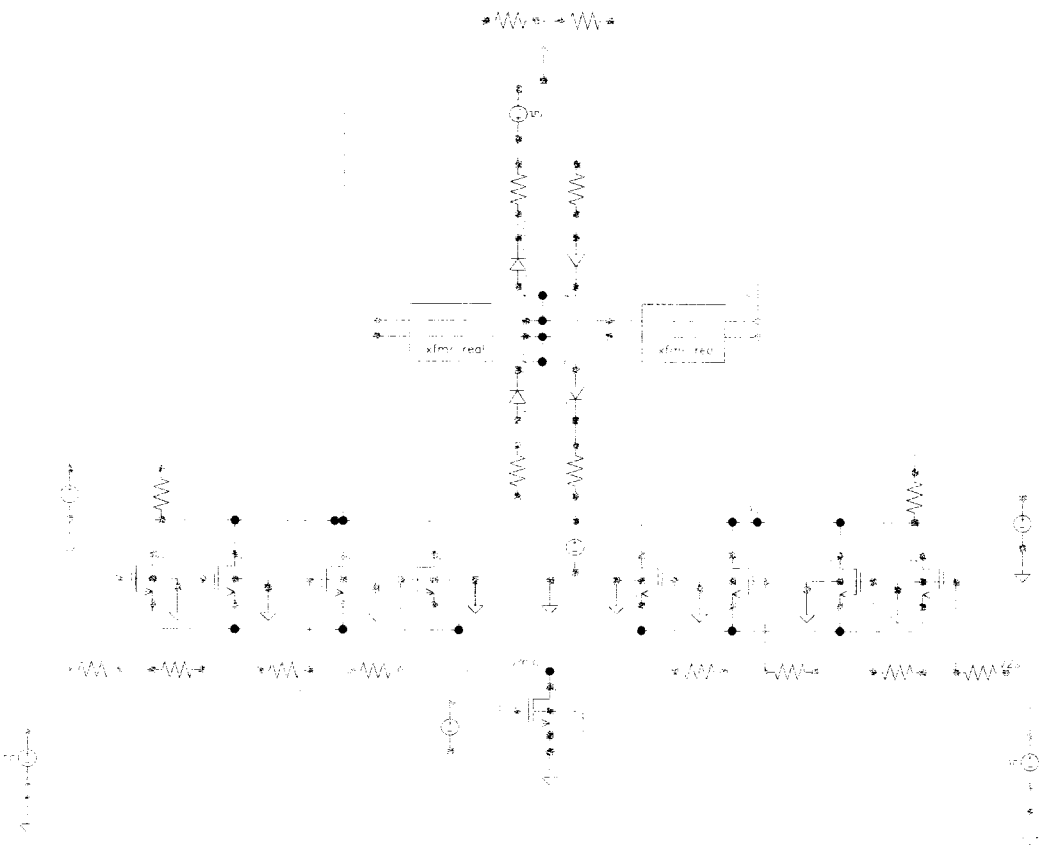

Figure 8.5 Schematic of the driver of the high speed serializer

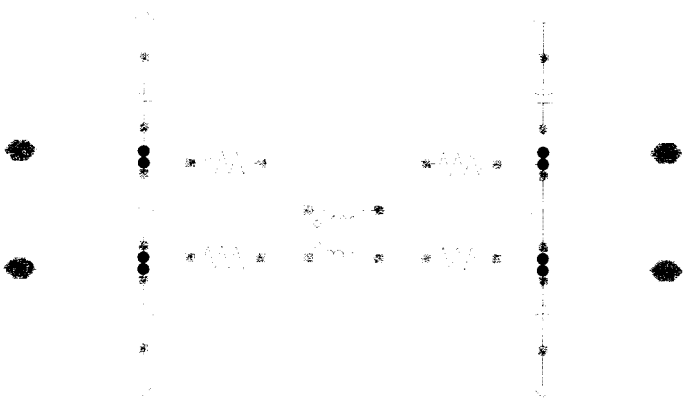

Figure 8.6 Transformer model in the driver

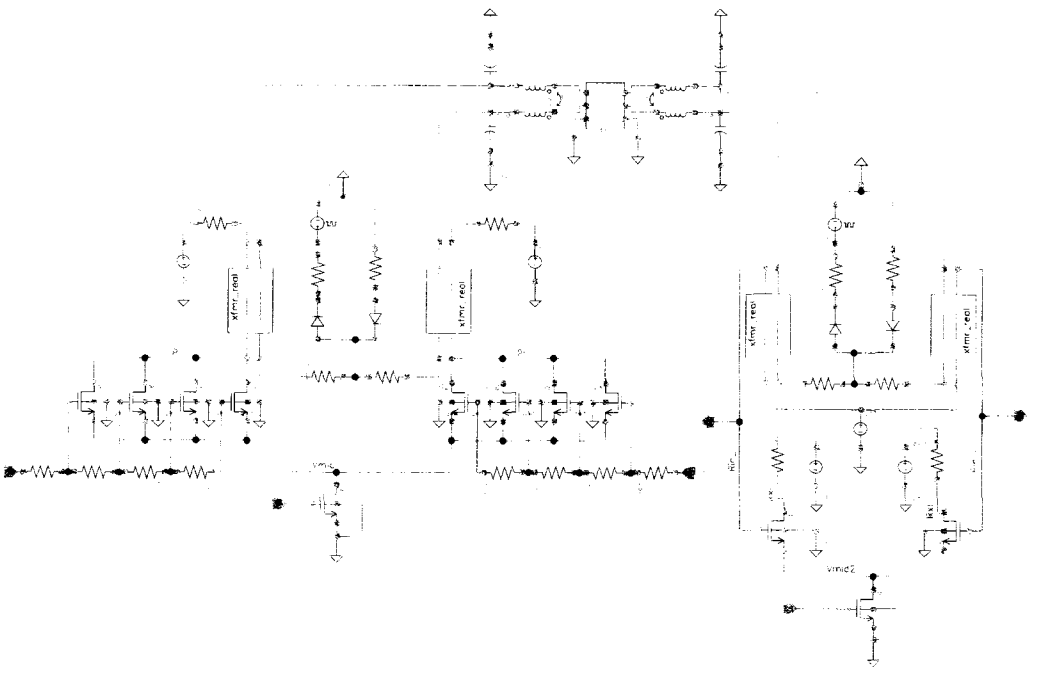

Figure 8.7 Driver and receiver front end schematic

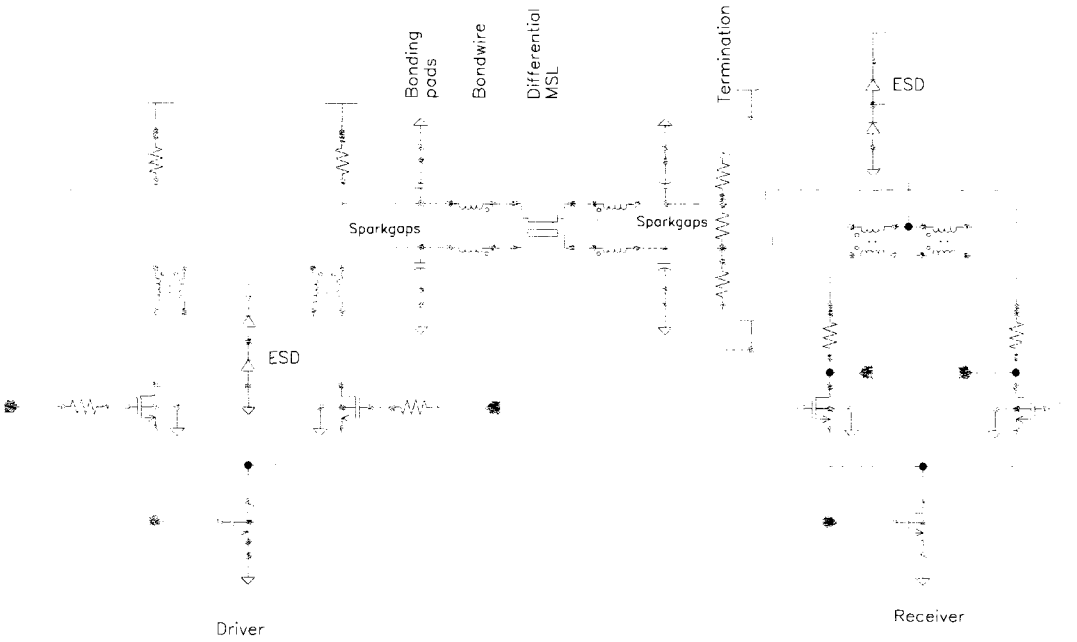

Figure 8.8 Transformer Isolation Scheme

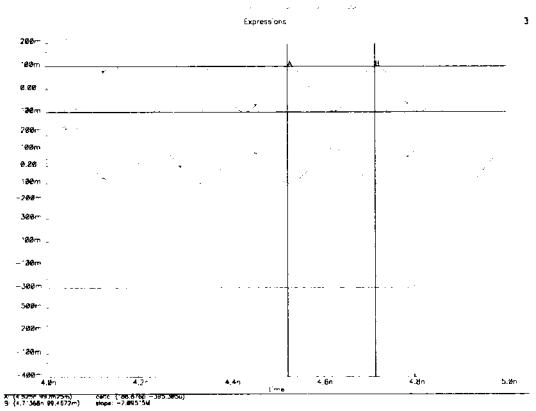

Figure 8.9 Transformer Isolation Scheme minimum bit rate

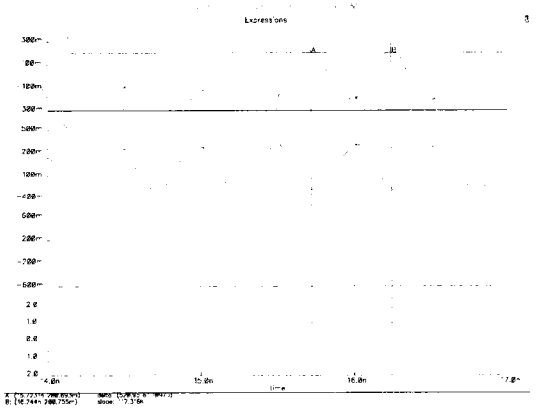

Figure 8.10 Transformer Isolation Scheme maximum bit rate

CHAPTER 9. Contribution summary

In this project several contributions were made. The following sections summarize them.

9.1 Geometric scaling

A method of characterization of RF inductors by geometric scaling was presented. The geometries of on chip passive RF components are scaled up by a factor α. The scaled model is characterized at a scaled down frequency range by a factor $1/\alpha$. The scattering parameters extracted from two geometrically scaled-up model at the scaled-down frequency range showed good agreement with the original on-chip inductors at the original desired frequency range. Extra parasitic capacitances that do not have any equivalence on-chip, reduced the effective inductance. The models gave also a lower bound for Q_{max} and $f_{Q_{max}}$ as compared to on-chip characterization results. This method can be utilized to give a prediction for RF spiral inductors before fabrication. While the equations given in Table 2.1 are primarily for lumped circuit elements, the same scale factor applies to distributed circuits, and work with distributed circuits will continue.

9.2 Transformer design and characterization in 0.18μ CMOS process

The contribution is the analysis, design, fabrication and characterization of monolithic RF transformers in 0.18μm CMOS process. Analysis is provided for 4 port ideal transformers. Several transformer structures were discussed such as planar interleaved transformers and proposed layout changes that have the potential for increasing the transformer coupling bandwidth. A ring transformer structure is introduced that allows less loss to be induced in the substrate. A software interface was developed for MATLAB, to help in designing a trans-

former in ASITIC. Recalibration and decoupling methods are presented too. Characterization results of the RF transformers agree with the design objective presented in this chapter. The resonance frequencies of 6 GHz for the transformers designed are higher than the bandwidth required 5 GHz.

9.3 Bandwidth improvement of toroidal transformers

Analysis of monolithic integrated transformers is presented. Several toroidal transformers were fabricated in 0.18μ CMOS process. Characterization results show a resonance frequency above 5GHz for the toroidal transformers with $|S_{13}| > 0.3$.

Other structures are developed where the parasitic capacitances, self or coupling, are minimized to maximize the resonance frequency of the transformer and improve its performance parameters. This structure depends on the concept of eliminating the overlap of top-bottom metal layers, and maximize the horizontal distance between the windings in the same layer to minimize the parasitic capacitances. The structures are intended to be fabricated in a custom ISU 2μ process.

9.4 Microstrip line modelling

A brief comparison study of GML1000 and FR4 materials for PCB circuits was provided. In this chapter it is proposed that GML1000 material be used over FR4 material for high speed circuits. This is due to the higher performance characteristics of the GML1000 material such as a stable ϵ_r over a larger frequency range, low loss factor, cost and compatibility with standard manufacturing process.

9.5 Bonding wire modelling toolbox in HSPICE and MATLAB

A bondwire modelling toolbox was developed for the case of Chip on Board assembly. The toolbox produces a circuit model that can be used in HSPICE simulation. The analysis shows that the level of impedance discontinuities in the BW decreases if the BW does not change the

height along its path from the PCB to the chip. If the BW is flat (ribbon) then the impedance variations can be greatly reduced.

9.6 RF and Gbit/s electrostatic discharge protection design

The contribution is a design of an RF and Gbit/s ESD structure using monolithic transformers and on-chip spark gaps. The design shows a protection level up to 10 kV for the HBM case, and 3 kV in the CDM case. The bandwidth of the device is from 1.5-6 GHz. A comparison of the results of the proposed ESD structure to existing state of the art RF ESD protection methods is presented in Table 7.1. The proposed methods prove, through simulations, to be competitive with other ESD protection methods.

9.7 Driver design and encoding scheme

In this chapter two encoding schemes for the driver are given for multilevel signaling. The first encoding scheme multiplexes the signal at the driver. The second scheme limits the number of variations in the outgoing signal. Several driver and receiver schemes are provided as schematic. The benchmark tests show that the driver can reach up to 10.6Gbit/s with a minimum bit rate of 3.8Gbit/s.

APPENDIX A. Planar transformer code

A.1 sweep1.m

```
    % Copyright © 2002
% Nader Badr
% All Rights Reserved


% This file will get the optimal coupling inductance

t1=clock;

len_min= ;      len_step= ;    len_max= ;
gap_min= ;      gap_step= ;     gap_max= ;
w_min= ;        w_step= ;      w_max= ;
s_min= ;        s_step= ;      s_max= ;
n1_min= ;       n1_step= ;      n1_max= ;
n2_min= ;       n2_step= ;      n2_max= ;
freq_min= ;     freq_step= ;    freq_max=5;
off_x= ;        off_y= ;      mtop1= ; mtop2= ; wg= ;

[st,hostname]=unix('hostname');

len_n=ceil((len_max-len_min)/len_step)+1;
w_n=ceil((w_max-w_min)/w_step)+1;
s_n=ceil((s_max-s_min)/s_step)+1;
n1_n=ceil((n1_max-n1_min)/n1_step)+1;
n2_n=ceil((n2_max-n2_min)/n2_step)+1;
gap_n=ceil((gap_max-gap_min)/gap_step)+1;



%lenx   =x(1);
%wx =x(2);
%sx =x(3);
addpath /constr

flag1=1;

t1=clock; number_of_points_left=len_n*w_n*s_n*n1_n*n2_n*gap_n;
elapsed_time=6; elapsed_times=6; k=1; k2=1;
LENI=1;GAP=1;SI=1;N1I=1;N2I=1; for leni=len_min:len_step:len_max,
    GAP=1;
    for gap=gap_min:gap_step:gap_max,
    WI=1;
    for wi=w_min:w_step:w_max,
    SI=1;
    for si=s_min:s_step:s_max,
        N1I=1;
        for n1i=n1_min:n1_step:n1_max,
            N2I=1;
```

```
for n2i=n2_min:n2_step:n2_max,


if(leni>(40+(4*ceil(n1i)*wi+(4*ceil(n1i)-2)*si)+2*wi) & 4000>pi*
(ceil(n1i)*leni)
& 30<pi*(ceil(n1i)*leni)),
                disp('-----------------------------------------------
                -------------')
    disp('.........................Start.............................')
    disp(['Simulation of M6 with NO GND in CMOS18 on ' hostname ' for '
    num2str(freq_min) ' GHz'])
                disp('-----------------------------------------------
                -------------')
                disp('.')
                disp('.')

            t0=clock;
                estimated_time_left=number_of_points_left*mean
                (elapsed_times)/60;
    number_of_points_left=number_of_points_left-1;
    disp(['len='num2str(leni) ' w=' num2str(wi) ' s=' num2str(si) ' n1='
    num2str(n1i) ' n2=' num2str(n2i)]);
    disp(['Time left is approximately ' num2str(ceil(estimated_time_left))
    ' minutes'])
                disp(['Average simulation time is ' num2str(mean
                (elapsed_times)
                /60) ' minutes'])
    disp(['Number of points left is ' num2str(number_of_points_left)])
    lens=leni-2*n1i*wi-2*(n1i-1)*si-2*gap;
    x=[leni wi si n1i lens n2i];
    [Mc,Fc,s12_m,s12_p,QL,fc_est]=tr_no_gnd_eval(x,off_x,off_y,mtop2,wg,
    freq_min,freq_step,freq_max);

        all_len(k2,2)   =leni;
        all_w(k2,2)     =wi;
        all_s(k2,2)     =si;
        all_n1(k2,2)        =n1i;
        all_n2(k2,2)        =n2i;
        all_Fc(k2,2)    =Fc;
        all_Mc(k2,2)    =Mc;
        all_s12_p(k2,2) =s12_p;
        all_s12_m(k2,2) =s12_m;
        all_QL(k2,2)    =QL;
        all_fc_est(k2,2)=fc_est;

        k2=k2+1;

        des_len(k,2)    =leni;
        des_w(k,2)      =wi;
        des_s(k,2)      =si;
        des_n(k,2)      =n1i;
        des_Fc(k,2)     =Fc;
        des_Mc(k,2)     =Mc;
        des_s12_p(k,2)  =s12_p;
        des_s12_m(k,2)  =s12_m;
        des_QL(k,2)     =QL;
        k=k+1;

            elapsed_times(flag1)=etime(clock,t0);
            disp(['Elapsed time for this simulation is   ' num2str(ceil
            (etime(clock,t0))) '   seconds'])
            elapsed_time=etime(clock,t0);
            flag1=flag1+1;
                disp('-----------------------------------------------
                -------------')
```

```
                disp('.............................END.............................')
                disp(['Simulation of M6 with NO GND in CMOS18 on ' hostname ' for '
                num2str(freq_min) ' GHz '])
                            disp('-----------------------------------------------
                            ------------')
                            disp('.')
                        save MMopt
            end

        N1I=N1I+1;
        end
        N2I=N2I+1;
        end
    SI=SI+1;
    end
    WI=WI+1;
    end
    GAP=GAP+1;
    end
    LENI=LENI+1;
end

elapsed_time=etime(clock,t1); disp(['Elapsed time for all
simulations is   ' num2str(ceil(etime(clock,t1)/60)) '
minutes']) save MMopt

pdata
```

A.2 tr_no_gnd_eval.m

```
    % Copyright © 2002
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function [Lps_c,FER_c,s12_mag,s12_ph,QL_c,fc_est] =
tr_no_gnd_eval(x,off_x,off_y,mtop,wg,freq_min,freq_step,freq_max)
% Sweep of inductor parameters for optimization


flag1   =1; k   =1; lenx    =x(1); leny    =x(5); wx  =x(2); sx
=x(3); nx  =x(4); ny  =x(6);



fn=1;  % number of frequency points
                t0=clock;


                    unix('date');
                    [a,b]=unix('rm tr_no_gnd.ip');
                    st=tr_no_gnd(lenx,leny,wx,sx,nx,ny,off_x,off_y,mtop,wg,freq_min,
                    freq_step,freq_max);
                    [a,b]=unix('cat tr_no_gnd.LOG > tr_no_gnd_tot.LOG');
                    [a,b]=unix('rm tr_no_gnd.LOG');
                    [a,b]=unix('rm sparam.dat');
                    com1='asitic_sun  ';
                    tekfile='-t CMOS18T.tek  ';
                    logfile='-l tr_no_gnd  ';
                    keyfile='-k tr_no_gnd.ip  ';
```

```
        disp(['Simulation of tr_no_gnd in CMOS18T on' unix('hostname')])
        disp(['len='num2str(lenx) ' w=' num2str(wx) ' s=' num2str(sx) '
        n=' num2str(nx)]);

        %unix([com1 tekfile logfile keyfile ]);
        unix([com1 tekfile logfile keyfile '-ng']);
        [Lmat,Cmat,coupling,zin]=get_data('home/nbadr/RESEARCH/ASITIC2/contr/
        tr_no_gnd.LOG',fn);

    nrows=size(Lmat,1);

    len(k:k+nrows-1,1)  =lenx;
    n1(k:k+nrows-1,1)   =nx;
    w(k:k+nrows-1,1)    =wx;
    s(k:k+nrows-1,1)    =sx;
    f(k:k+nrows-1,1)    =Lmat(:,1);
    QL1(k:k+nrows-1,1)  =Lmat(:,2);
    QL2(k:k+nrows-1,1)  =Lmat(:,3);
    QLd(k:k+nrows-1,1)  =Lmat(:,4);
    L(k:k+nrows-1,1)    =Lmat(:,5);
    LR(k:k+nrows-1,1)   =Lmat(:,6);
    LCs1(k:k+nrows-1,1) =Lmat(:,7);
    LRs1(k:k+nrows-1,1) =Lmat(:,8);
    LCs2(k:k+nrows-1,1) =Lmat(:,9);
    LRs2(k:k+nrows-1,1) =Lmat(:,10);
    FER(k:k+nrows-1,1)  =Lmat(:,11);

    QC1(k:k+nrows-1,1)  =Cmat(:,2);
    QC2(k:k+nrows-1,1)  =Cmat(:,3);
    QCd(k:k+nrows-1,1)  =Cmat(:,4);
    C(k:k+nrows-1,1)    =Cmat(:,5);
    CR(k:k+nrows-1,1)   =Cmat(:,6);
    CCs1(k:k+nrows-1,1) =Cmat(:,7);
    CRs1(k:k+nrows-1,1) =Cmat(:,8);
    CCs2(k:k+nrows-1,1) =Cmat(:,9);
    CRs2(k:k+nrows-1,1) =Cmat(:,10);

    Lpp(k:k+nrows-1,1)  =coupling(:,1);
    Rpp(k:k+nrows-1,1)  =coupling(:,2);
    Lps(k:k+nrows-1,1)  =coupling(:,3);
    Rps(k:k+nrows-1,1)  =coupling(:,4);
    Lss(k:k+nrows-1,1)  =coupling(:,5);
    Rss(k:k+nrows-1,1)  =coupling(:,6);

    zin_r(k:k+nrows-1,1)    =zin(:,1);
    zin_im(k:k+nrows-1,1)   =zin(:,2);


    k=k+nrows;
    elapsed_times(flag1)=etime(clock,t0);
    %disp(['Elapsed time for this simulation is   ' num2str(ceil(etime
    (clock,t0)/60)) '   minutes'])

    elapsed_time=etime(clock,t0);
    flag1=flag1+1;
save tr_no_gnd.mat
disp('Fix_data.................')
[L_c,Lps_c,FER_c,QL_c,fc_est]=fix_data('tr_no_gnd');
disp('READ_SPAR.................')
[s12_mag,s12_ph]=read_spar('sparam.dat');

save tr_no_gnd.mat
```

A.3 tr_no_gnd.m

```
    % Copyright © 2002
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function
st=tr_no_gnd(len1,len2,w,s,n1,n2,off_x,off_y,mtop,wg,freq_min,freq_step,freq_max)

fid1=fopen('tr_no_gnd.ip','w');

fprintf(fid1,'# Spiral with flux path transformer Input file to
ASITIC\n'); fprintf(fid1,'# 2 spirals on top of each other. Return
path through lower inductor\n');
fprintf(fid1,'# Generated on %s\n',datestr(now,-1));
fprintf(fid1,'# by Nader Badr  \n\n\n\n'); fprintf(fid1,'set
snap_size=.02  \n');

% th =theta
%ri= ;                  % Inner loop
%s= ;                   % Spacing between rio and roi
%tw= ;                  % Width of segments in transformer winding radius
%d= ;                   % Thickness of the metal layer
%seg_i= ;               % Segment number starts with 1
%nx= ;                  % Number of vias in the x direction
%ny= ;                  % Number of vias in the y direction
%mbot= ;                % Bottom metal layer
off_x=off_x-len1/2;     % x offset
off_y=off_y-len1/2;     % y offset
%ni= ;                  % Number of turns
%mtop= ;                % Top metal layer
%wg= ;                  % width of ground conductor
% Inner loop ------------------------------------------------------


fprintf(fid1,'square\np1\n%i\n%6.2f\n%6.2f\n%4.2f\nCM%i\ny\nCM%i\nc\n',len1,w,
s,n1,mtop,mtop-1);
fprintf(fid1,'square\ns1\n%i\n%6.2f\n%6.2f\n%4.2f\nCM%i\ny\nCM%i\nc\n',len2,w,
s,n2,mtop,mtop-1);

fprintf(fid1,'wire\ngnd\n5\n5\nCM%i\n1\nc\n0\n',mtop);


%status=gnd(fid1,len_gnd,w,xorg,yorg);

% -------------------------SIMULATION-----------------------------------------
----------



for freq=freq_min:freq_step:freq_max
    fprintf(fid1,'# sim_frequency=%4.1f\n',freq);
    fprintf(fid1,'pic p1 s1 %i gnd \n',freq);
    fprintf(fid1,'k2 %i p1 s1 \n',freq);

end

fprintf(fid1,'2porttrans p1 s1 gnd %i %i %i\n',freq_min,freq_max,freq_step);
fprintf(fid1,'exit\n');

st=fclose(fid1);
```

A.4 get_data.m

```
    % Copyright © 2002
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function [Lmat,Cmat,coupling,zin]=get_data(filename,fn)

% Open the file for read mode
% To extract data from it

fid = fopen(filename,'r');
% Read one line at a time
sim=1; row=1;
 f=zeros(fn,1);
 QL1=zeros(fn,1);
 QL2=zeros(fn,1);
 QLd=zeros(fn,1);
 L=zeros(fn,1);
 LR=zeros(fn,1);
 LCs1=zeros(fn,1);
 LRs1=zeros(fn,1);
 LCs2=zeros(fn,1);
 LRs2=zeros(fn,1);
 FER=zeros(fn,1);

 f=zeros(fn,1);
 QC1=zeros(fn,1);
 QC2=zeros(fn,1);
 QCd=zeros(fn,1);
 C=zeros(fn,1);
 CR=zeros(fn,1);
 CCs1=zeros(fn,1);
 CRs1=zeros(fn,1);
 CCs2=zeros(fn,1);
 CRs2=zeros(fn,1);
 Lpp=zeros(fn,1);
 Rpp=zeros(fn,1);
 Lps=zeros(fn,1);
 Rps=zeros(fn,1);
 Lss=zeros(fn,1);
 Rss=zeros(fn,1);
 zin_r=zeros(fn,1);
 zin_im=zeros(fn,1);


while feof(fid)==0
        line = fgetl(fid);
        line=[line blanks(2)];

        ind2x= findstr(line,'Pi Model at f=');
        if(isempty(ind2x)==0 & ind2x ~=0),

            linek = fgetl(fid);

            % find the frequency of operation
            % --------------------------------
            ind_Hz=findstr(line,'Hz');
            ind3x=ind2x+length('Pi Model at f=');

            % check if the colon is included in the string
            line2x=line(ind3x:ind_Hz-2);

            if(line(ind_Hz-1)~=' '),
```

```
f(row,1)=str2num(line2x)*mulfac(line(ind_Hz-1));
else
f(row,1)=str2num(line2x);
end


if(linek(1:2)=='C='),

    % Find the QC factor
    ind4x= findstr(line,'Q =');

    line4x=line(ind4x+4:max(length(line)));
    ind_cm=findstr(line4x,',');
    % find QL for port 1
    % ---------------------------------
    q1_tmp = str2num(line4x(1:ind_cm(1)-2));
    % check for multiplication factor
    if(line4x(ind_cm(1)-1)~=' '),
        QC1(row,1)=  mulfac(line4x(ind_cm(1)-1))*q1_tmp;
    else
        QC1(row,1)=  q1_tmp;
        QL1(row,1)=  0;
    end
    % find Q for port 2
    % ---------------------------------
    q2_tmp = str2num(line4x(ind_cm(1)+2:ind_cm(2)-2));
    if(line4x(ind_cm(2)-1)~=' '),
        QC2(row,1)=  mulfac(line4x(ind_cm(2)-1))*q2_tmp;
    else
        QC2(row,1)=  q2_tmp;
        QL2(row,1)=  0;
    end
    % find Q differential
    % ---------------------------------
    % look for the space before the multiplication factor if any
    ind_dq=findstr(line4x(ind_cm(2)+2:max(length(line4x))),' ');
    qd_tmp = str2num(line4x(ind_cm(2)+2:ind_cm(2)+ind_dq(1)));

    % check if there is a multiplication factor
    line4x(ind_cm(2)+ind_dq(1)+2);
    if(line4x(ind_cm(2)+ind_dq(1)+2)~=' '),
        % There's a multiplication factor
        QCd(row,1)=  mulfac(line4x(ind_cm(2)+ind_dq(1)+2))*qd_tmp;
    else
        % No multiplication factor
        QCd(row,1)=  qd_tmp;
        QLd(row,1)=  0;
    end

    indC=findstr(linek,'F');
    C(row,1)=str2num(linek(3:indC-2))*mulfac(linek(indC-1));
    L(row,1)=0;

    ind_R=findstr(linek,'R');
    line1=[line(ind_R+2:max(length(linek))) blanks(3)];
    ind_rf=findstr(line1,' ');


    % Read the third line to get Cs1 and Rs1
    linek = fgetl(fid);
    ind_Cs1=findstr(linek,'F');
    CCs1(row,1)=str2num(linek(6:ind_Cs1-2))*mulfac(linek(ind_Cs1-1
    :ind_Cs1-1));
    LCs1(row,1)=0;

    ind_Rs1=findstr(linek,'Rs1=');
```

```
        line1=[linek(ind_Rs1+4:max(length(linek))) blanks(3)];
        ind_rf=findstr(line1,' ');

        if(line1(ind_rf(1)+1)~=' '),
            CRs1(row,1)=str2num(line1(1:ind_rf(1)-1))*mulfac(line1(
            ind_rf(1)+1:ind_rf(1)+1));
            LRs1(row,1)=0;
        else
            linexyz=line1(1:ind_rf(1)-1);
            CRs1(row,1)=str2num(line1(1:ind_rf(1)-1));
            LRs1(row,1)=0;
        end


        % Read the fourth line to get Cs2 and Rs2 and Resonance Frequency
        linek = fgetl(fid);
        ind_Cs2=findstr(linek,'F');
        CCs2(row,1)=str2num(linek(6:ind_Cs2-2))*mulfac(linek(ind_Cs2-1:
        ind_Cs2-1));
        LCs2(row,1)=0;

        ind_Rs2=findstr(linek,'Rs2=');
        line1=linek(ind_Rs2+4:max(length(linek)));
        ind_rf=findstr(line1,' ');


    end



    flag2=1;
    %save test1.mat


end


ind2x= findstr(line,'L(p1,p1) = ');
if(isempty(ind2x)==0 & ind2x ~=0),

    ind_Hz=findstr(line,'H');
    line2x=line(11:ind_Hz-2);
    if(line(ind_Hz-1)~=' '),
    Lpp(row,1)=str2num(line2x)*mulfac(line(ind_Hz-1));
    else
    Lpp(row,1)=str2num(line2x);
    end

    ind_R=findstr(line,'R(p1,p1) =');
    line1=[line(ind_R+11:max(length(line))) blanks(3)];
    ind_rf=findstr(line1,' ');

    if(line1(ind_rf(1)+1)~=' '),
        Rpp(row,1)=str2num(line1(1:ind_rf(1)-1))*mulfac(line1(ind_rf(1)+1));
    else
        Rpp(row,1)=str2num(line1(1:ind_rf(1)-1));
    end

    line = fgetl(fid);
    ind_Hz=findstr(line,'H');
    line2x=line(11:ind_Hz-2);
    if(line(ind_Hz-1)~=' '),
    Lps(row,1)=str2num(line2x)*mulfac(line(ind_Hz-1));
    else
    Lps(row,1)=str2num(line2x);
    end
```

```
    ind_R=findstr(line,'R(p1,s1) =');
    line1=[line(ind_R+11:max(length(line))) blanks(3)];
    ind_rf=findstr(line1,' ');

    if(line1(ind_rf(1)+1)~=' '),
        Rps(row,1)=str2num(line1(1:ind_rf(1)-1))*mulfac(line1(ind_rf(1)+1));
    else
        Rps(row,1)=str2num(line1(1:ind_rf(1)-1));
    end

    line = fgetl(fid);
    ind_Hz=findstr(line,'H');
    line2x=line(11:ind_Hz-2);
    if(line(ind_Hz-1)~=' '),
    Lss(row,1)=str2num(line2x)*mulfac(line(ind_Hz-1));
    else
    Lss(row,1)=str2num(line2x);
    end

    ind_R=findstr(line,'R(s1,s1) =');
    line1=[line(ind_R+11:max(length(line))) blanks(3)];
    ind_rf=findstr(line1,' ');

    if(line1(ind_rf(1)+1)~=' '),
        Rss(row,1)=str2num(line1(1:ind_rf(1)-1))*mulfac(line1(ind_rf(1)+1));
    else
        Rss(row,1)=str2num(line1(1:ind_rf(1)-1));
    end


 end

 ind2x= findstr(line,'Zin = ');
 if(isempty(ind2x)==0 & ind2x ~=0),
    ind2_nan=findstr(line,'nan');
    if(isempty(ind2_nan)==1 | ind2_nan ==0),
        ind_im=findstr(line,'+ j');
        line2x=line(7:ind_im-2);
        if(line(ind_im-1)~=' '),
            zin_r(row,1)=str2num(line2x)*mulfac(line(ind_im-1));
        else
            zin_r(row,1)=str2num(line2x);
        end

        line2x=deblank(line(ind_im+3:max(size(line))));
        maxl=max(size(line2x));
        mulf=line2x(maxl);

        if(isempty(str2num(mulf))==1),
            zin_im(row,1)=str2num(line2x(1:maxl-1))*mulfac(line2x(maxl));
        else
            zin_im(row,1)=str2num(line2x(1:maxl));
        end

        flag2=1;
        row=row+1;
else
 zin_r(row,1)=0;
 zin_im(row,1)=0;

end

 end
```

```
end


Lmat    =[f QL1 QL2 QLd L LR LCs1 LRs1 LCs2 LRs2 FER]; Cmat    =[f
QC1 QC2 QCd C CR CCs1 CRs1 CCs2 CRs2 ]; coupling=[Lpp Rpp Lps Rps
Lss Rss]; zin =[zin_r zin_im];

fclose(fid);
```

A.5 fix_data.m


```
function [L_c,Lps_c,FER_c,QL1_c,fc_est] = fix_data(filename)

p1=1; p2=40; nc=50;

eval(['load ' filename '.mat'])


              len_c       = len ;
              w_c         =   w ;
              s_c         =   s ;
              n_c         =   n1 ;

              f_c         =   f ;
              QL1_c       = QL1 ;
              QL2_c       = QL2 ;
              QLd_c       = QLd ;
              L_c         =   L ;
              LR_c        =  LR ;
              LCs1_c      =LCs1 ;
              LRs1_c      =LRs1 ;
              LCs2_c      =LCs2 ;
              LRs2_c      =LRs2 ;
              FER_c       = FER ;

              QC1_c       = QC1 ;
              QC2_c       = QC2 ;
              QCd_c       = QCd ;
              C_c         =   C ;
              CR_c        =  CR ;
              CCs1_c      =CCs1 ;
              CRs1_c      =CRs1 ;
              CCs2_c      =CCs2 ;
              CRs2_c      =CRs2 ;

              Lpp_c       =Lpp ;
              Rpp_c       =Rpp ;
              Lps_c       =Lps ;
              Rps_c       =Rps ;
              Lss_c       =Lss ;
              Rss_c       =Rss ;

              zin_r_c     =zin_r ;
              zin_i_c     =zin_im ;
```

```
                zin_c       =(zin_r_c  +i*zin_i_c  );
                zin_mag_c   =abs(zin_r_c  +i*zin_i_c  );
                zin_ph_c    =(phase((zin_r_c  +i*zin_i_c  )'))';
                fc_est      =1/(2*pi*sqrt(Lps_c*C_c));

    %end

flag=0; eval(['save ' filename 'a.mat'])
```

A.6 read_spar.m

```
    % Copyright © 2002
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function [s12_mag,s12_ph]=read_spar(filename)


% filename is sparam.dat
%matlab('load' filename 'a.mat len_c w_c s_c n_c Lpp_c Lps_c Lss_c FER_c QL1_c L_c'])



% Open the file for read mode
% To extract data from it

fid = fopen(filename,'r');
% Read one line at a time
k=1; nb=1; while feof(fid)==0
        line = fgetl(fid);
        line=[line blanks(2)];
        ind2x= findstr(line,'# HZ S MA');
        if(isempty(ind2x)==0 & ind2x ~=0),
        for n=1:nb,
                line = fgetl(fid);
                mall(k,:)   =str2num(line);
            k=k+1;
        end
    end
end

        freq(   1,1)        =mall(1,1)*1e-9;
        s11_mag(1,1)        =mall(1,2);
        s11_ph( 1,1)        =mall(1,3);
        s12_mag(1,1)        =mall(1,4);
        s12_ph(1,1)     =mall(1,5);
        if(s12_ph==nan),
            s12_ph(1,1)=-1;
        end
        s21_mag(1,1)        =mall(1,6);
        s21_ph( 1,1)        =mall(1,7);
        s22_mag(1,1)        =mall(1,8);
        s22_ph( 1,1)        =mall(1,9);



fclose(fid);
```

A.7 pdata.m

```
    % Copyright © 2002
% Nader Badr
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load  MMopt Mc1=1.3e-9; fres=15e9; Qth=.1;
disp('=====================================CASE1=========================
=============
') disp('index all_l   all_w   all_s   all_n1 all_n2   all_Fc
all_Mc all_QL all_s12_m all_s12_p  all_fc_est')

format short e for kk=1:size(all_w,1)

    if(all_Mc(kk,2)>Mc1),

        disp([num2str(kk) ' ' num2str(all_len(kk,2)) '  ' num2str
        (all_w(kk,2)) '    '...
        num2str(all_s(kk,2))  ' ' num2str(all_n1(kk,2))  '  ' num2str(
        all_n2(kk,2))  '  ' ...
        num2str(all_Fc(kk,2))  '    ' num2str(all_Mc(kk,2)) '   ' ...
        num2str(all_QL(kk,2)) ' ' ...
        num2str(all_s12_m(kk,2))  ' ' num2str(all_s12_p(kk,2)) '    '
        num2str(all_fc_est(kk,2),'%0.5g')])
    end

end



disp('=====================================CASE2=========================
==============
') disp('index all_l   all_w   all_s   all_n   all_Fc  all_Mc
all_QL all_s12_m all_s12_p ') for kk=1:size(all_w,1)

    if(all_Mc(kk,2)>Mc1 & all_Fc(kk,2)>fres & all_QL(kk,2)>Qth), %  & all_s
    (kk,2)>3 ),

        disp([num2str(kk) ' ' num2str(all_len(kk,2)) '  ' num2str(all_w
        (kk,2)) '    '...
        num2str(all_s(kk,2))  ' ' num2str(all_n(kk,2))  '   ' ...
        num2str(all_Fc(kk,2))  '    ' num2str(all_Mc(kk,2)) '   ' ...
        num2str(all_QL(kk,2)) ' ' ...
        num2str(all_s12_m(kk,2))  ' ' num2str(all_s12_p(kk,2))  '   '
        num2str(all_fc_est(kk,2),'%0.5g')])
    end

end
```

APPENDIX B. Toroidal transformer code

B.1 solen5x.m

```
    % Copyright © 2002
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fid1=fopen(['s5.inp'],'w');

fprintf(fid1,'# Toroidal Solenoid transformer Input file to
ASITIC\n');
fprintf(fid1,'# Generated on %s\n',datestr(now,-1));
fprintf(fid1,'# by Nader Badr  \n\n\n\n');

% th =theta
N= ;            % N= number of vertical loops in the toroid
rax= ;          % Inner radius of toroid from inner edge of winding
rbx= ;          % Outer radius of toroid from outer edge of winding
tw= ;           % width of segments in transformer winding
d= ;            % thickness of the metal layer
seg_i= ;        % segment number starts with 1
nx= ;           % number of vias in the x direction
ny= ;           % number of vias in the y direction
mtop= ;         % Top metal layer
mbot= ;         % Bottom metal layer
via= ;          % via
off_x= ;        % x offset
off_y= ;        % y offset

for th=2*pi/N:2*pi/N:2*pi
        th1a=th;
        th2a=th+pi/N;
        ra=rax+tw/2;
        rb=rbx-tw/2;

        ssina=(rbx*sin(th2a)-rax*sin(th1a));
        scosa=(rbx*cos(th2a)-rax*cos(th1a));

        if(ssina>=0 & scosa>=0)
            thm1a=atan(ssina/scosa);
        elseif(ssina>=0 & scosa<=0)
            thm1a=pi+atan(ssina/scosa);
        elseif(ssina<=0 & scosa<=0)
            thm1a=pi+atan(ssina/scosa);
        elseif(ssina<=0 & scosa>=0)
            thm1a=2*pi+atan(ssina/scosa);
        end
        cmxa=(rbx*cos(th2a)+rax*cos(th1a))/2; % center of wire x value
        cmya=(rbx*sin(th2a)+rax*sin(th1a))/2; % center of wire y value
        lena=sqrt((rbx*sin(th2a)-rax*sin(th1a))^2+(rbx*cos(th2a)-rax*
        cos(th1a))^2); % length of wire
```

```
delxa=tw/2*(sin(thm1a)-cos(thm1a));
delya=tw/2*(-sin(thm1a)-cos(thm1a));
rmxa=off_x+cmxa-lena/2;  % XORG
rmya=off_y+cmya-tw/2;   % YORG

% Inner via
if(th<2*pi),
    fprintf(fid1,'# Segment number is %i\n',seg_i);
    %fprintf(fid1,'# Thm1=%6.2f \t Th1=%6.2f \t Th2=%6.2f \n',thm1
    *180/pi,th1*180/pi,th2*180/pi);
    %fprintf(fid1,'# delx=%6.2f \t dely=%6.2f \n',delx,dely);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,lena,tw,mtop,rmxa,rmya,
    180/pi*thm1a,1);
    if(seg_i>1),
        fprintf(fid1,'join r1 r%i  \n\n',seg_i);
    end
    seg_i=seg_i+1;
    % Vias on the inner perimeter of the toroid

    for num=mbot:mtop-1
        fprintf(fid1,'# Connection between vias %i\n',seg_i);
        %fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
        xorg=%6.4e:
        yorg=%6.4e:orient=0:phase=%i\n', ...
        %seg_i,tw*1.1,tw*1.1,num,off_x+rax*cos(th1a)-tw/2,off_y+rax
        *sin(th1a)-tw/2,-1);
        seg_i=seg_i+1;

        %fprintf(fid1,'# Via number is %i\n',seg_i);
        %fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',
        seg_i,num,nx,ny,off_x+rax*cos(th1a),off_y+rax*sin(th1a));
        seg_i=seg_i+1;

        fprintf(fid1,'join r%i r%i \n',seg_i-2,seg_i-1);
    end

    %fprintf(fid1,'# Via number is %i\n',seg_i);
    %fprintf(fid1,'via\nvx%i\nCV%i\n%i\n%i\n1\n%6.4e  %6.4e\n\n',seg_i,
    mbot,mtop,nx,ny,200+rax*cos(th1),200+rax*sin(th1));
    %fprintf(fid1,'join w1 vx%i  \n\n',seg_i);

    seg_i=seg_i+1;
end
% Outer vias going up
if(th<(2*pi-2*pi/N)),
     for num=mbot:mtop-1
        fprintf(fid1,'# Connection between vias %i\n',seg_i);
        %fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
        xorg=%6.4e:yorg=%6.4e:orient=0:phase=%i\n', ...
    %    seg_i,tw*1.2,tw*1.2,num,off_x+rbx*cos(th2a)-tw/2,off_y+rbx*
    sin(th2a)-tw/2,-1);
        seg_i=seg_i+1;

        %fprintf(fid1,'# Via number is %i\n',seg_i);
        %fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n1\n%6.4e  %6.4e\n\n',
        seg_i,num,nx,ny,off_x+rbx*cos(th2a),off_y+rbx*sin(th2a));
        seg_i=seg_i+1;

        fprintf(fid1,'join r%i r%i \n',seg_i-2,seg_i-1);
        %fprintf(fid1,'# Connection between vias %i\n',seg_i);
        %fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
        xorg=%6.4e:yorg=%6.4e:orient=0:phase=%i\n', ...
     %   seg_i,tw*1.2,tw*1.2,num+1,off_x+rbx*cos(th2a)-tw/2,off_y+
     rbx*sin(th2a)-tw/2,-1);
        seg_i=seg_i+1;
```

```
            end
        elseif(th==(2*pi-2*pi/N)),
            fprintf(fid1,'# Wire extension number is %i\n',seg_i);
            fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
            yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,lena,tw,mtop,off_x+rbx*
            cos(th2a),off_y+rbx*sin(th2a)-tw/2,0,1);
            fprintf(fid1,'join r1 r%i  \n\n',seg_i);
            seg_i=seg_i+1;
        elseif(th==2*pi),
             for num=mbot:mtop-1
                %fprintf(fid1,'# Connection between vias %i\n',seg_i);
                %fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
                xorg=%6.4e:yorg=%6.4e:orient=0:phase=%i\n', ...
                %seg_i,tw*1.2,tw*1.2,num,off_x+rbx*cos(th2a)-tw/2,off_y+rbx*
                sin(th2a)-tw/2,-1);
                seg_i=seg_i+1;

                %fprintf(fid1,'# Via number is %i\n',seg_i);
                %fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n1\n%6.4e  %6.4e\n\n',
                seg_i,num,nx,ny,off_x+rbx*cos(th2a),off_y+rbx*sin(th2a));
                seg_i=seg_i+1;

                fprintf(fid1,'join r%i r%i \n',seg_i-2,seg_i-1);

                %fprintf(fid1,'# Connection between vias %i\n',seg_i);
                %fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
                xorg=%6.4e:yorg=%6.4e:orient=0:phase=%i\n', ...
            %    seg_i,tw*1.2,tw*1.2,num+1,off_x+rbx*cos(th2a)-tw/2,off_y+
            rbx*sin(th2a)-tw/2,-1);
                seg_i=seg_i+1;
            end

            fprintf(fid1,'# Wire extension number is %i\n',seg_i);
            fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
            yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,lena,tw,mtop,off_x+
            rbx*cos(th2a),off_y+rbx*sin(th2a)-tw/2,0,-1);
            fprintf(fid1,'join r1 r%i  \n\n',seg_i);
            seg_i=seg_i+1;
        end

%end

%for th=2*pi/N:2*pi/N:2*pi
        th1b=th;
        th2b=th-pi/N;
        ra=rax+tw/2;
        rb=rbx-tw/2;

        ssinb=(rbx*sin(th2b)-rax*sin(th1b));
        scosb=(rbx*cos(th2b)-rax*cos(th1b));

        if(ssinb>=0 & scosb>=0)
            thm1b=atan(ssinb/scosb);
        elseif(ssinb>=0 & scosb<=0)
            thm1b=pi+atan(ssinb/scosb);
        elseif(ssinb<=0 & scosb<=0)
            thm1b=pi+atan(ssinb/scosb);
        elseif(ssinb<=0 & scosb>=0)
            thm1b=2*pi+atan(ssinb/scosb);
        end
        cmxb=(rbx*cos(th2b)+rax*cos(th1b))/2; % center of wire x value
        cmyb=(rbx*sin(th2b)+rax*sin(th1b))/2; % center of wire y value
        lenb=sqrt((rbx*sin(th2b)-rax*sin(th1b))^2+(rbx*cos(th2b)-rax*
        cos(th1b))^2); % length of wire
        rmxb=off_x+cmxb-lenb/2;  % XORG
        rmyb=off_y+cmyb-tw/2;   % YORG
```

```
        if(th<2*pi)
            fprintf(fid1,'# Segment number is %i\n',seg_i);
            %fprintf(fid1,'# Thm1=%6.2f \t Th1=%6.2f \t Th2=%6.2f \n',
            thm1*180/pi,th1*180/pi,th2*180/pi);
            %fprintf(fid1,'# delx=%6.2f \t dely=%6.2f \n',delx,dely);
            fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
            yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,lenb,tw,mbot,rmxb,
            rmyb,180/pi*thm1b,-1);
            fprintf(fid1,'join r1 r%i  \n\n',seg_i);
            seg_i=seg_i+1;
        end

end
for x=2:seg_i-1
    fprintf(fid1,'join r1 r%i \n',x);
end

fprintf(fid1,'set save_matrix=true\n');
%fprintf(fid1,'SaveMat=true\n');
%fprintf(fid1,'pix r1 .5\n');
for freq=1:1:0
    %fprintf(fid1,'# sim_frequency=%4.1f\n',freq);
    %fprintf(fid1,'pix r1 %i\n',freq);
end

fprintf(fid1,'exit\n');


fclose(fid1);

grid on
```

B.2 square98.m

```
    % Copyright © 2002
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function []=square98(N,r1,w,s,dy)


fid1=fopen(['s1.i'],'w');

fprintf(fid1,'# Toroidal Solenoid transformer Input file to
ASITIC\n');
fprintf(fid1,'# Generated on %s\n',datestr(now,-1));
fprintf(fid1,'# by Nader Badr  \n\n\n\n'); fprintf(fid1,'grid
\n'); fprintf(fid1,'set snap_size=.01  \n');

% Input values

% N= ;           % number of loops primar. Must be a multiple of 4
% r1= ;          % Inner width of loop in pri or sec
% w= ;      % width of the interconnect
d= ;          % thickness of the metal layer
% s= ;      % Spacing of pri-pri and pri-sec
gap= ;      % Spacing of Between loops on the edges
mtop= ;         % Top metal layer
mbot= ;         % Bottom metal layer
via= ;          % via
xoff= ;   % x offset
```

```
yoff= ;   % y offset
% dy= ;

% Inner values

W1 =r1+2*w  % Width of the loop from outside edge to outside edge
L1a=4*w+3*s;    % length of inner connection from one winding to
                % the other
L1b=2*w+s;      % length of outer connection from one winding to
                % the other

W2 =r1+2*w  % Width of the loop from outside edge to outside edge
L2a=2*w+s;  % length of inner connection from one winding to
            % the other
L2b=4*w+3*s;% length of outer connection from one winding to
            % the other
L3a=(dy-(N/4-1)*(s+L1a)-s)/2;

seg_i=1;        % segment number starts with 1
nx=1;           % number of vias in the x direction
ny=1;           % number of vias in the y direction
L3a=(dy-(N/4-1)*(s+L1a)-s)/2;

seg_i=1;

% Right Leg-----------------------------------------------------------------
-------------------------------------------------------------------------

totd=dy+W1+s-w -2*(w+s)   +W1+s+w;

%  xoffst + left leg + gap + lower leg
xo=xoff   + (W1+s+w)  + L3a + (L1a+s)*N/4 +225;
% xo=0;yo=0
%  yoff  + lower leg
yo=yoff  + (W1+s+w) -2*(w+s) +225  ; totd=dy+W1+s-w -2*(w+s)
+W1+s+w; cpx=totd/2+450/2; cpy=cpx;

xo=cpx+dy/2-s-2*w; yo=cpy-dy/2; for i=1:N/4

    if i==1,

        fprintf(fid1,'# Segment number is %i\n',seg_i);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
        xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,
        L3a-w-s,mtop,xo,yo+w+s,0,0);
    else
        fprintf(fid1,'# Segment number is %i\n',seg_i);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
        xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,
        L1a,mtop,xo,yo+(i-2)*(L1a+s)+(L3a+s),0,0);
    end

    seg_i=seg_i+1;

    fprintf(fid1,'# Segment number is %i\n',seg_i);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
    xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,W1,w,
    mtop,xo,yo+(i-2)*(L1a+s)+(L3a+s)+L1a-w,0,0);

    seg_i=seg_i+1;

    fprintf(fid1,'# Via number is %i\n',seg_i);
    fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',
    seg_i,mbot,nx,ny,xo+W1-w/2,yo+(i-2)*(L1a+s)+(L3a+s)+L1a-w/2);

    seg_i=seg_i+1;
```

```
    fprintf(fid1,'# Segment number is %i\n',seg_i);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
    xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,L1b,
    mbot,xo+W1-w,yo+(i-2)*(L1a+s)+(L3a+s)+L1a-w,0,0);

    seg_i=seg_i+1;

    fprintf(fid1,'# Segment number is %i\n',seg_i);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
    xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,W1,w,
    mbot,xo,yo+(i-2)*(L1a+s)+(L3a+s)+L1a+s,0,0);

    seg_i=seg_i+1;

    fprintf(fid1,'# Via number is %i\n',seg_i);
    fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',
    seg_i,mbot,nx,ny,xo+w/2,yo+(i-1)*(L1a+s)+(L3a+s)+w/2);

    seg_i=seg_i+1;

    for x=seg_i-6:seg_i-1
        fprintf(fid1,'join r1 r%i \n',x);
    end

    if i==N/4,
        fprintf(fid1,'# Segment number is %i\n',seg_i);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
        xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,
        L3a-w-s,mtop,xo,yo+(i-1)*(L1a+s)+(L3a+s),0,0);

        seg_i=seg_i+1;

        fprintf(fid1,'# Via number is %i\n',seg_i);
        fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',
        seg_i,mbot,nx,ny,xo+w/2,yo+(i-1)*(L1a+s)+(L3a+s)+w/2);

        seg_i=seg_i+1;

        for x=seg_i-2:seg_i-1
            fprintf(fid1,'join r1 r%i \n',x);
        end
    end


end




seg_j=seg_i;

% Right Leg-----------------------------------------OUTER---------------
-------------------------------------------------------
%  xoffst   left leg + gap  + lower leg
% xo=xoff  + (W1+s+w)+L3a + (L1a+s)*N/4;

%  yoff  + lower leg + gap
% yo=yoff  + (W1+s+w) + L3a  ;

for j=1:N/4

    if j==1
        fprintf(fid1,'# Segment number is %i\n',seg_j);
```

```
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
    xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,
    L3a-(w+s),mbot,xo+w+s,yo,0,0);
else
    fprintf(fid1,'# Segment number is %i\n',seg_j);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:
    xorg=%6.4e:yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,
    L2a,mbot,xo+w+s,yo+(j-2)*(L1a+s)+(L3a+s)+w+s,0,0);
end

seg_j=seg_j+1;

fprintf(fid1,'# Segment number is %i\n',seg_j);
fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,W1,w,mbot,xo+w+s,yo+(j-2)
*(L1a+s)+(L3a+s)+w+s+L2a-w,0,0);

seg_j=seg_j+1;

fprintf(fid1,'# Via number is %i\n',seg_j);
fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_j,
mbot,nx,ny,xo+s+W1+w/2,yo+(j-2)*(L1a+s)+(L3a+s)+L1a-3/2*w-s);

seg_j=seg_j+1;


fprintf(fid1,'# Segment number is %i\n',seg_j);
fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,L2b,mtop,xo+W1+s,yo+(j-2)
*(L1a+s)+(L3a+s)+2*(w+s),0,0);

seg_j=seg_j+1;

fprintf(fid1,'# Segment number is %i\n',seg_j);
fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,W1,w,mtop,xo+w+s,yo+(j-2)*
(L1a+s)+(L3a+s)+L1a+2*s+w,0,0);

seg_j=seg_j+1;

fprintf(fid1,'# Via number is %i\n',seg_j);
fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_j,mbot,
nx,ny,xo+w+s+w/2,yo+(j-2)*(L1a+s)+(L3a+s)+L1a+2*s+w+w/2);

seg_j=seg_j+1;

for x=seg_j-6:seg_j-1
    fprintf(fid1,'join r1 r%i \n',x);
end

if j==N/4,
    fprintf(fid1,'# Segment number is %i\n',seg_j);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e
    :yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,L3a-w-s,mbot,xo+w+s,
    yo+(j-1)*(L1a+s)+(L3a+s)+w+s,0,0);

    seg_j=seg_j+1;

    for x=seg_j-2:seg_j-1
        fprintf(fid1,'join r1 r%i \n',x);
    end


end
```

```
end


% Left Leg-------------------------------------------------------------------
--------------------------------------------------------------------------------
%  xoffst   left leg   + lower leg
% xo=xoff  + (W1+s+w);

%  yoff  + lower leg + gap
% yo=yoff  + (W1+s+w) + L3a  ;

fprintf(fid1,'cp r1 r2 \n'); fprintf(fid1,'rotate r2 180\n');

dx=W1+s+w; dy=2*L3a+(N/4-1)*(s+L1a)+s;

fprintf(fid1,'move r2 %6.4e 0\n',-dy-W1-s+w +2*(w+s));

fprintf(fid1,'join r1 r2\n'); fprintf(fid1,'cp r1 s1\n');

fprintf(fid1,'rotate s1 90\n'); fprintf(fid1,'join r1 s1\n');

totd=dy+W1+s-w -2*(w+s)   +W1+s+w;
% fprintf(fid1,'move r1 %6.4e %6.4e\n',-dy-W1-s+w +2*(w+s),-W1-s-w);
% fprintf(fid1,'move r1 %6.4e %6.4e\n',totd/2,totd/2);

% ------------------------------------------------   PADS    ----------
-----------------------------------------------------------------------

    fprintf(fid1,'# Segment number is 1\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',1,75,75,mtop,xoff+225+totd/2-137.5,
    yoff+50,0,0);

    fprintf(fid1,'# Segment number is 2\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',2,75,75,mtop,xoff+225+totd/2-37.5,
    yoff+50,0,0);

    fprintf(fid1,'# Segment number is 3\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',3,75,75,mtop,xoff+225+totd/2+62.5,
    yoff+50,0,0);
% ------------------------------------------------   GND CENTRL    -----
-----------------------------------------------------------------------

    fprintf(fid1,'# Segment number is 4\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',4,10,60,mtop,xoff+225+totd/2-105,
    yoff,0,0);

    fprintf(fid1,'# Segment number is 5\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',5,10,60,mtop,xoff+225+totd/2+95,
    yoff,0,0);

    fprintf(fid1,'# Segment number is 6\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',6,210,10,mtop,xoff+225+totd/2-105,
    yoff,0,0);
% ------------------------------------------------   GND CENTRL    -----
-----------------------------------------------------------------------

    fprintf(fid1,'# Segment number is 7\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',7,15+225+totd/2-100-87.5,30,mtop,
```

```
    xoff+72.5,yoff+72.5,0,0);

    fprintf(fid1,'# Segment number is 8\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',8,15+225+totd/2-100-87.5,30,mtop,
    xoff+225+totd/2+100,yoff+72.5,0,0);

% ------------------------------------------------  SUB CONTACTS    -------
-----------------------------------------------------------------
    fprintf(fid1,'# Segment number is 9\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',9,20,20,1,xoff+77.5,yoff+77.5,0,0);

    fprintf(fid1,'# Segment number is 10\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',10,20,20,1,xoff+450+totd-97.5,
    yoff+77.5,0,0);

        for x=2:10
             fprintf(fid1,'join p1 p%i \n',x);
        end

fprintf(fid1,'cp p1 q1\n'); fprintf(fid1,'flipH q1\n');
fprintf(fid1,'move q1 0 %6.4e\n',totd+325);
fprintf(fid1,'join p1 q1\n'); fprintf(fid1,'cp p1 q1\n');
fprintf(fid1,'rotate q1 90\n'); fprintf(fid1,'join p1 q1\n');
fprintf(fid1,'join r1 p1\n');
fprintf(fid1,'rename r1 N%i_R%i_W%i_S%i_D%i\n',N,r1,w,s,dy);
fprintf(fid1,'cifsave N%i_R%i_W%i_S%i_D%i  N%i_R%i_W%i_S%i_D%i.cif\n',
N,r1,w,s,dy,N,r1,w,s,dy);
%fprintf(fid1,'exit');

fclose(fid1);

com1='asitic_sun  -8'; tekfile='-t MRC.tek  '; logfile='-l
ASITIClog  '; keyfile='-k s1.i ';

unix([com1 tekfile logfile keyfile ]);
```

B.3 squares.m

```
    % Copyright © 2002
% Nader Badr
% All Rights Reserved


function []=squares(N,r1,w,s,dy)


fid1=fopen(['s1.i'],'w');

fprintf(fid1,'# Toroidal Solenoid transformer Input file to
ASITIC\n');
fprintf(fid1,'# Generated on %s\n',datestr(now,-1));
fprintf(fid1,'# by Nader Badr  \n\n\n\n'); fprintf(fid1,'grid
\n'); fprintf(fid1,'set snap_size=.01  \n');

% Input values

% N= ;              % number of loops primar. Must be a multiple of 4
% r1= ;             % Inner width of loop in pri or sec
% w= ;              % width of the interconnect
```

```
d= ;                % thickness of the metal layer
% s= ;              % Spacing of pri-pri and pri-sec
gap= ;              % Spacing of Between loops on the edges
mtop= ;             % Top metal layer
mbot= ;             % Bottom metal layer
via= ;              % via
xoff= ;             % x offset
yoff= ;             % y offset
% dy= ;

% Inner values

W1 =r1+2*w  % Width of the loop from outside edge to outside edge
L1a=4*w+3*s;    % length of inner connection from one winding to
        % the other
L1b=2*w+s;      % length of outer connection from one winding to
        % the other

W2 =r1+2*w  % Width of the loop from outside edge to outside edge
L2a=2*w+s;  % length of inner connection from one winding to
        % the other
L2b=4*w+3*s;    % length of outer connection from one winding to
        % the other
L3a=(dy-(N/4-1)*(s+L1a)-s)/2;

seg_i=1;        % segment number starts with 1
nx=1;           % number of vias in the x direction
ny=1;           % number of vias in the y direction
L3a=(dy-(N/4-1)*(s+L1a)-s)/2;

seg_i=1;

% Right Leg-----------------------------------------------------------
-------------------------------------------------------------------------

totd=dy+W1+s-w -2*(w+s)   +W1+s+w;

%  xoffst + left leg + gap + lower leg
xo=xoff   + (W1+s+w)  + L3a + (L1a+s)*N/4 +225;
% xo=0;yo=0
%  yoff  + lower leg
yo=yoff  + (W1+s+w) -2*(w+s) +225  ; totd=dy+W1+s-w -2*(w+s)
+W1+s+w; cpx=totd/2+450/2; cpy=cpx;

xo=cpx+dy/2-s-2*w; yo=cpy-dy/2; for i=1:N/4

    if i==1,

        fprintf(fid1,'# Segment number is %i\n',seg_i);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
        yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,L3a-w-s,mtop,xo,yo+w+s,0,0);
    else
        fprintf(fid1,'# Segment number is %i\n',seg_i);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
        yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,L1a,mtop,xo,yo+(i-2)*(
        L1a+s)+(L3a+s),0,0);
    end

    seg_i=seg_i+1;

    fprintf(fid1,'# Segment number is %i\n',seg_i);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,W1,w,mtop,xo,yo+(i-2)*(L1a+s)
    +(L3a+s)+L1a-w,0,0);

    seg_i=seg_i+1;
```

```
    fprintf(fid1,'# Via number is %i\n',seg_i);
    fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_i,
    mbot,nx,ny,xo+W1-w/2,yo+(i-2)*(L1a+s)+(L3a+s)+L1a-w/2);

    seg_i=seg_i+1;


    fprintf(fid1,'# Segment number is %i\n',seg_i);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,L1b,mbot,xo+W1-w,yo+(i-2)*
    (L1a+s)+(L3a+s)+L1a-w,0,0);

    seg_i=seg_i+1;

    fprintf(fid1,'# Segment number is %i\n',seg_i);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,W1,w,mbot,xo,yo+(i-2)*(L1a+s)
    +(L3a+s)+L1a+s,0,0);

    seg_i=seg_i+1;

    fprintf(fid1,'# Via number is %i\n',seg_i);
    fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_i,mbot,nx,
    ny,xo+w/2,yo+(i-1)*(L1a+s)+(L3a+s)+w/2);

    seg_i=seg_i+1;

    for x=seg_i-6:seg_i-1
        fprintf(fid1,'join r1 r%i \n',x);
    end

    if i==N/4,
        fprintf(fid1,'# Segment number is %i\n',seg_i);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
        yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_i,w,L3a-w-s,mtop,xo,yo+(i-1)*
        (L1a+s)+(L3a+s),0,0);

        seg_i=seg_i+1;

        fprintf(fid1,'# Via number is %i\n',seg_i);
        fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_i,mbot,
        nx,ny,xo+w/2,yo+(i-1)*(L1a+s)+(L3a+s)+w/2);

        seg_i=seg_i+1;

        for x=seg_i-2:seg_i-1
            fprintf(fid1,'join r1 r%i \n',x);
        end
    end


end




seg_j=seg_i;

% Right Leg-----------------------------------------OUTER-----------------
-------------------------------------------------
%  xoffst   left leg + gap  + lower leg
% xo=xoff  + (W1+s+w)+L3a + (L1a+s)*N/4;

%  yoff  + lower leg + gap
```

```
% yo=yoff  + (W1+s+w) + L3a  ;

for j=1:N/4

    if j==1
        fprintf(fid1,'# Segment number is %i\n',seg_j);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
        yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,L3a-(w+s),mtop,xo+w+s,yo,0,0);
    else
        fprintf(fid1,'# Segment number is %i\n',seg_j);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
        yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,L2a,mtop,xo+w+s,yo+(j-2)*
        (L1a+s)+(L3a+s)+w+s,0,0);
    end

    seg_j=seg_j+1;

    fprintf(fid1,'# Segment number is %i\n',seg_j);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,W1,w,mtop,xo+w+s,yo+(j-2)*
    (L1a+s)+(L3a+s)+w+s+L2a-w,0,0);

    seg_j=seg_j+1;

    fprintf(fid1,'# Via number is %i\n',seg_j);
    fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_j,mbot,
    nx,ny,xo+s+W1+w/2,yo+(j-2)*(L1a+s)+(L3a+s)+L1a-3/2*w-s);

    seg_j=seg_j+1;


    fprintf(fid1,'# Segment number is %i\n',seg_j);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,L2b,mbot,xo+W1+s,yo+(j-2)*
    (L1a+s)+(L3a+s)+2*(w+s),0,0);

    seg_j=seg_j+1;

    fprintf(fid1,'# Segment number is %i\n',seg_j);
    fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,W1,w,mbot,xo+w+s,yo+(j-2)*
    (L1a+s)+(L3a+s)+L1a+2*s+w,0,0);

    seg_j=seg_j+1;

    fprintf(fid1,'# Via number is %i\n',seg_j);
    fprintf(fid1,'via\nr%i\nCV%i\n%i\n%i\n-1\n%6.4e  %6.4e\n\n',seg_j,
    mbot,nx,ny,xo+w+s+w/2,yo+(j-2)*(L1a+s)+(L3a+s)+L1a+2*s+w+w/2);

    seg_j=seg_j+1;

    for x=seg_j-6:seg_j-1
        fprintf(fid1,'join r1 r%i \n',x);
    end

    if j==N/4,
        fprintf(fid1,'# Segment number is %i\n',seg_j);
        fprintf(fid1,'wire name=r%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
        yorg=%6.4e:orient=%6.4e:phase=%i\n',seg_j,w,L3a-w-s,mtop,xo+w+s,yo+
        (j-1)*(L1a+s)+(L3a+s)+w+s,0,0);

        seg_j=seg_j+1;

        for x=seg_j-2:seg_j-1
            fprintf(fid1,'join r1 r%i \n',x);
        end
```

```
    end


end

% Left Leg-------------------------------------------------------------
-------------------------------------------------------------------------
%  xoffst   left leg   + lower leg
% xo=xoff  + (W1+s+w);

%  yoff  + lower leg + gap
% yo=yoff  + (W1+s+w) + L3a  ;

fprintf(fid1,'cp r1 r2 \n'); fprintf(fid1,'rotate r2 180\n');

dx=W1+s+w; dy=2*L3a+(N/4-1)*(s+L1a)+s;

fprintf(fid1,'move r2 %6.4e 0\n',-dy-W1-s+w +2*(w+s));

fprintf(fid1,'join r1 r2\n'); fprintf(fid1,'cp r1 s1\n');

fprintf(fid1,'rotate s1 90\n'); fprintf(fid1,'join r1 s1\n');

totd=dy+W1+s-w -2*(w+s)   +W1+s+w;
% fprintf(fid1,'move r1 %6.4e %6.4e\n',-dy-W1-s+w +2*(w+s),-W1-s-w);
% fprintf(fid1,'move r1 %6.4e %6.4e\n',totd/2,totd/2);

% ------------------------------------------------   PADS    ---------
-------------------------------------------------------------------------

    fprintf(fid1,'# Segment number is 1\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',1,75,75,mtop,xoff+225+totd/2-137.5,
    yoff+50,0,0);

    fprintf(fid1,'# Segment number is 2\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',2,75,75,mtop,xoff+225+totd/2-37.5,
    yoff+50,0,0);

    fprintf(fid1,'# Segment number is 3\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',3,75,75,mtop,xoff+225+totd/2+62.5,
    yoff+50,0,0);
% ------------------------------------------------   GND CENTRL    ----
-------------------------------------------------------------------------

    fprintf(fid1,'# Segment number is 4\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',4,10,60,mtop,xoff+225+totd/2-105,
    yoff,0,0);

    fprintf(fid1,'# Segment number is 5\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',5,10,60,mtop,xoff+225+totd/2+95,
    yoff,0,0);

    fprintf(fid1,'# Segment number is 6\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',6,210,10,mtop,xoff+225+totd/2-105,
    yoff,0,0);
% ------------------------------------------------   GND CENTRL    --
```

```
-----------------------------------------------------------------------

    fprintf(fid1,'# Segment number is 7\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',7,15+225+totd/2-100-87.5,30,mtop,
    xoff+72.5,yoff+72.5,0,0);

    fprintf(fid1,'# Segment number is 8\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',8,15+225+totd/2-100-87.5,30,mtop,
    xoff+225+totd/2+100,yoff+72.5,0,0);

% ------------------------------------------------   SUB CONTACTS
  ------------------------------------------------------------------------
    fprintf(fid1,'# Segment number is 9\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',9,20,20,1,xoff+77.5,yoff+77.5,0,0);

    fprintf(fid1,'# Segment number is 10\n');
    fprintf(fid1,'wire name=p%i:len=%6.4e:w=%6.4e:metal=CM%i:xorg=%6.4e:
    yorg=%6.4e:orient=%6.4e:phase=%i\n',10,20,20,1,xoff+450+totd-97.5,
    yoff+77.5,0,0);

        for x=2:10
             fprintf(fid1,'join p1 p%i \n',x);
        end

fprintf(fid1,'cp p1 q1\n'); fprintf(fid1,'flipH q1\n');
fprintf(fid1,'move q1 0 %6.4e\n',totd+325);
fprintf(fid1,'join p1 q1\n'); fprintf(fid1,'cp p1 q1\n');
fprintf(fid1,'rotate q1 90\n'); fprintf(fid1,'join p1 q1\n');
fprintf(fid1,'join r1 p1\n');
fprintf(fid1,'rename r1 SN%i_R%i_W%i_S%i_D%i\n',N,r1,w,s,dy);
fprintf(fid1,'cifsave SN%i_R%i_W%i_S%i_D%i  SN%i_R%i_W%i_S%i_D%i.cif\n',
N,r1,w,s,dy,N,r1,w,s,dy);
%fprintf(fid1,'exit');

fclose(fid1);

com1='asitic_sun  '; tekfile='-t MRC.tek  '; logfile='-l
ASITIClog'; keyfile='-k s1.i';

unix([com1 tekfile logfile keyfile ]);
```

APPENDIX C. Bond wire code

C.1 gen2m.m

```
    % Copyright © 2001
% Nader Badr
% All Rights Reserved


% This file generates rlgc models of the several cases of bondwire segments
% All the model files generated by HSPICE are written in one file seg.rlgc

% Enter geometry of the bondwire

% (x0,y0) coordinates of point in middle of pcb pad
% (x1,y1) coordinates of point by edge of pcb pad
% (x2,y2) coordinates of point close to chip pad ( turn point)
% (x3,y3) coordinates of point in middle of chip pad
% The more points the better
% Written by Nader Badr Spring 2001
function gen2m(run) fidn=fopen(['bw_tot2.hsp'],'w');
fid2=fopen(['bw_sub.lib'],'w');
fprintf(fid2,'* Complete Bond
wiremodel input file to HSPICE\n');
fprintf(fid2,'* Generated on %s\n',datestr(now,-1));
fprintf(fid2,'* by Nader Badr  \n\n\n\n');

% Specify length of segment ~ 2*diameter of wire
%seg_len=bw_diam*2;


condc =      ;          fprintf(fid2,'* condc=%4.2e \t\tConductivity of chip
metal\n',condc);
condp =      ;          fprintf(fid2,'* condp=%4.2e \t\tConductivity of pcb
metal\n',condp);
condbw =      ;         fprintf(fid2,'* condbw=%4.2e \t\tConductivity of
bondwire\n',condbw);
erc=   ;                fprintf(fid2,'* erc=%4.2e m \t\tDielectric constant of
material \n',erc);
erp=    ;               fprintf(fid2,'* erp=%4.2e m \t\tDielectric constant of
material of pcb\n',erp);
hc=      ;              fprintf(fid2,'* hc=%4.2e m \t\tThickness of dielectric
layer of chip \n',hc);
hp=      ;              fprintf(fid2,'* hp=%4.2e m \t\tThickness of dielectric
layer of pcb \n',hp);
ltc =      ;            fprintf(fid2,'* ltc=%4.2e \t\t\tLoss tangent \n',ltc);
ltp =      ;            fprintf(fid2,'* ltp=%4.2e \t\t\tLoss tangent \n',ltp);
pc=       ;             fprintf(fid2,'* pc=%4.2e m \t\tExtension of chip bondpad
under bondwire \n',pc);
pp=       ;             fprintf(fid2,'* pp=%4.2e m \t\tExtension of pcb bondpad
under bondwire \n',pp);
rad =     ;             fprintf(fid2,'* rad=%4.2e m \t\tRadius of bondwire \n',rad);
```

```
spacep= ;         fprintf(fid2,'* spacep=%4.2e m \t\tDistance from
pad_edge_inner to pad_edge_inner
 at pcb pad_center\n',spacep);
spacec= ;          fprintf(fid2,'* sspcec=%4.2e m \t\tDistance from
pad_edge_inner to pad_edge_inner
 at chip pad_center\n',spacec);
tc=      ;              fprintf(fid2,'* tc=%4.2e m \t\tThickness of bondpad
of chip \n',tc);
tg=      ;              fprintf(fid2,'* tg=%4.2e m \t\tThickness of gnd
plane of pcb \n',tg);
tp=      ;              fprintf(fid2,'* tp=%4.2e m \t\tThickness of bondpad
 of pcb \n',tp);
wc=      ;              fprintf(fid2,'* wc=%4.2e m \t\tWidth of bondpad
of chip \n',wc);
wp=      ;              fprintf(fid2,'* wp=%4.2e m \t\tWidth of bondpad
of pcb \n',wp);
msl_len= ;


% Generate function of bw height

nop=100;  % number of points generated
x=[0    tc;
   25   tc;
   225 (.7*(hc+tc));
   425 (tc);
   450 (tc)];
x(:,2)=x(:,2)+1*rad; cc=x(:,2); x(:,1)=x(:,1)*1e-6;
maxdis=x(max(size(x,1)),1);
%figure(1),plot(x(:,1),x(:,2),'b-')

sp2=spline(x(:,1),x(:,2));
xx=linspace(0,maxdis,nop)';
d=ppval(sp2,xx)+tg+hp+tp+rad;
coord=[xx d];
%figure(2),plot(xx,d,'b-')
%hold on
%figure(2),stairs(xx,d,'r-')

len=maxdis/nop;
fprintf(fid2,'* len=%4.2e m \t\tLength of segment of line \n',len);

d=d ;
fprintf(fid2,'* d  \t\t\t\tHeight of bondwire from
gnd\n\n');
%break

% Generate position of bondwires as a function of distance

spc=wc+spacec; spp=wp+spacep; cl=.5*(wp+spp);

% slope
m=(spc-spp)./(xx(nop)-xx(1)); s=m*xx+spp; pos1=cl-s/2;
pos2=cl+s/2;


% Create pads


fprintf(fidn,'\n\n\n\n.LIB
''/home/nbadr/RESEARCH/channel1/gml_bondwire/bw_sub.lib''  bw1
\n');
fprintf(fidn,'\n\n.inc
''/home/nbadr/RESEARCH/channel1/gml_bondwire/msl.rlgc''     \n');
fprintf(fidn,'.OPTIONS
SEARCH=''/home/nbadr/RESEARCH/channel1/gml_bondwire/  ''\n');
```

```
fprintf(fidn,'  .OPTION PROBE POST\n');
fprintf(fidn,'  +ACCURA
\n');
fprintf(fidn,'  +METHOD=GEAR\n');
fprintf(fidn,'  +ABSMOS =
1.00000E-12\n');
fprintf(fidn,'  +RELV   = 1.00000E-06\n');
fprintf(fidn,'  +ABSI   = 1.00000E-14\n');
fprintf(fidn,'  +ABSV
= 1.00000E-03\n');
fprintf(fidn,'  +CO = 132\n');
fprintf(fidn,'
+INGOLD = 2\n');
fprintf(fidn,'  +TLINLIMIT=1\n');
fprintf(fidn,'
+DELMAX=.001n\n\n\n');

fprintf(fidn,'I1 nc1a nc1b AC=0mA DC=0  pulse(0mA 5mA 0 .05n .05n
.18 0.5)\n');
%fprintf(fidn,'Ix node1 gnd pulse(0 -.5nA  0 .499n .0005n .00025n .5n) \n');
%fprintf(fidn,'.AC LIN 200 1MHz 10GHz\n\n');
%fprintf(fid2,'Rx node1 gnd 1k\n');



!rm seg.rlgc !rm msl.rlgc flp=0; fld=0; flc=0;
fprintf(fid2,'.LIB
bw1\n\n');
fprintf(fid2,'.SUBCKT bw1 na%i nb%i na%i nb%i\n',1,1,nop+1,nop+1);
fprintf(fid2,'\n\n.inc
''/home/nbadr/RESEARCH/channel1/gml_bondwire/seg.rlgc''     \n');
fprintf(fidn,'X1 na%i nb%i na%i nb%i bw1\n',1,1,nop+1,nop+1);

fprintf(fid2,'Ra1 na1 nc1 1e-5\n');
fprintf(fid2,'Rb1 nb1 nd1
1e-5\n\n');


% msl

disp(['seg=' num2str(0) '   msl_o_pcb'])
msl_o_pcb(0,condc,condbw,condp,d(1),erc,erp,hc,hp,msl_len,ltc,ltp,pc,pp,
rad,pos1(1),pos2(1),tc,tg,tp,wc,wp);

fprintf(fidn,'W%i na%i nb%i gnd na%i nb%i gnd\n',0,0,0,1,1);
fprintf(fidn,'+RLGCmodel=segmodel_%i N=2 l=%4.2e\n\n',0,msl_len);
        if(run==0)
            %!nice hspice bw_seg.sp > bw_seg.out
        else
            !nice hspice bw_seg.sp > bw_seg.out
        end
        !rm *.tr0
        !rm *.out
        !cp bw_seg.sp bw_segmsl.sp
        !rm bw_seg.sp
        !rm *.ic
        !rm *.st0

%break

for nd=1:nop,

   % for segments close to pcb pad
   if (xx(nd)<= wp/2)
      disp(['seg=' num2str(nd) '   bw_o_pcbpad'])
        fprintf(fid2,'* pos1=%4.2e \t\t\t\tPosition of  bw1_center from pcb
```

```
    pad side\n',pos1(nd));
    fprintf(fid2,'* pos2=%4.2e \t\t\t\tPosition of  bw2_center from pcb
    pad side\n',pos2(nd));

  bw_o_pcbpad(nd,condc,condbw,condp,d(nd),erc,erp,hc,hp,len,ltc,ltp,pc,
  pp,rad,pos1(nd),pos2(nd),tc,tg,tp,wc,wp);

  % Generate hspice rlgc file that contains the spice elements
    %!mv *.sp bw_seg.sp
    if(run==0)
        %!nice hspice bw_seg.sp > bw_seg.out
    else
        !nice hspice bw_seg.sp > bw_seg.out
    end
    !rm *.tr0
    !rm *.out
    !cp bw_seg.sp bw_segp.sp
    !rm bw_seg.sp
    !rm *.ic
    !rm *.st0
    clear fid
    % Write the model in bw_tot.sp

    fprintf(fid2,'W%i na%i nb%i nc%i nd%i gnd na%i nb%i nc%i nd%i gnd\n',
    nd,nd,nd,nd,nd,nd+1,nd+1,nd+1,nd+1);
    fprintf(fid2,'+RLGCmodel=segmodel_%i N=4 l=%4.2e\n\n',nd,len);
    flp=1;


elseif(xx(nd)> wp/2 & xx(nd)< (maxdis-wc/2))

   if(flp==1)
    fprintf(fid2,'Ra%i nc%i gnd 100G\n',nd,nd);
    fprintf(fid2,'Rb%i nd%i gnd 100G\n\n',nd,nd);
    flp=0;
   end


   disp(['seg=' num2str(nd) '   bw_o_diel'])

    fprintf(fid2,'* pos1=%4.2e \t\t\t\tPosition of  bw1_center from pcb
    pad side\n',pos1(nd));
    fprintf(fid2,'* pos2=%4.2e \t\t\t\tPosition of  bw2_center from pcb
    pad side\n',pos2(nd));

  bw_o_diel(nd,condc,condbw,condp,d(nd),erc,erp,hc,hp,len,ltc,ltp,pc,pp,
  rad,pos1(nd),pos2(nd),tc,tg,tp,wc,wp);

    % Generate hspice rlgc file that contains the spice elements
    %!mv *.sp bw_seg.sp
    %!nice hspice bw_seg.sp > bw_seg.out
    if(run==0)
        %!nice hspice bw_seg.sp > bw_seg.out
    else
        !nice hspice bw_seg.sp > bw_seg.out
    end
    !rm *.tr0
    !rm *.out
    !cp bw_seg.sp bw_segd.sp
    !rm bw_seg.sp
    !rm *.ic
    !rm *.st0
    clear fid
    % Write the model in bw_tot.sp

    fprintf(fid2,'W%i na%i nb%i gnd na%i nb%i gnd\n',nd,nd,nd,nd+1,nd+1);
```

```
      fprintf(fid2,'+RLGCmodel=segmodel_%i N=2 l=%4.2e\n\n',nd,len);
    fld=1;

    elseif(xx(nd)>= (maxdis-wc/2))
     if(fld==1)
      fprintf(fid2,'Ra%i nc%i gnd 100G\n',nd,nd);
      fprintf(fid2,'Rb%i nd%i gnd 100G\n\n',nd,nd);
      fld=0;
     end

    disp(['seg=' num2str(nd) '   bw_o_chippad'])
      fprintf(fid2,'* pos1=%4.2e \t\t\t\tPosition of  bw1_center from pcb
      pad side\n',pos1(nd));
      fprintf(fid2,'* pos2=%4.2e \t\t\t\tPosition of  bw2_center from pcb
      pad side\n',pos2(nd));

      bw_o_chippad(nd,condc,condbw,condp,d(nd),erc,erp,hc,hp,len,ltc,ltp,
      pc,pp,rad,pos1(nd),pos2(nd),tc,tg,tp,wc,wp);

      % Generate hspice rlgc file that contains the spice elements
      %!mv *.sp bw_seg.sp
      %!nice hspice bw_seg.sp > bw_seg.out
      if(run==0)
          %!nice hspice bw_seg.sp > bw_seg.out
      else
          !nice hspice bw_seg.sp > bw_seg.out
      end
      !rm *.tr0
      !rm *.out
      !cp bw_seg.sp bw_segc.sp
      !rm bw_seg.sp
      !rm *.ic
      !rm *.st0
      clear fid
      % Write the model in bw_tot.sp

      fprintf(fid2,'W%i na%i nb%i nc%i nd%i gnd na%i nb%i nc%i nd%i gnd\n',
      nd,nd,nd,nd,nd,nd+1,nd+1,nd+1,nd+1);
      fprintf(fid2,'+RLGCmodel=segmodel_%i N=4 l=%4.2e\n\n',nd,len);

  end


end



fprintf(fid2,'Ra%i na%i nc%i 1e-5\n',nd+1,nd+1,nd+1);
fprintf(fid2,'Rb%i nb%i nd%i 1e-5\n\n',nd+1,nd+1,nd+1);
fprintf(fid2,'.ENDS bw1 \n\n'); fprintf(fid2,'.ENDL bw1 \n\n');
fclose(fid2);


fprintf(fidn,'X2 na%i nb%i naa%i nbb%i bw1\n',0,0,0,0);


fprintf(fidn,'.NET v(na%i,nb%i) I1 ROUT=121.467 RIN=121.467\n',nd+1,nd+1);
fprintf(fidn,'.PRINT AC S11(R) S11(I) S12(R) S12(I) S21(R) S21(I)
S22(R) S22(I)\n'); fprintf(fidn,'.PRINT AC S11(DB) S11(P) S12(DB)
S12(P) S21(DB) S21(P) S22(DB) S22(P)\n'); fprintf(fidn,'.PRINT AC
\n\n'); fprintf(fidn,'.END \n');

fclose(fidn);


% Draw pcb gnd layer
```

```
axis([xx(1)-.2e-3   1.3*xx(nop)   -pos2(1)   2*pos2(1)   0
max(d)])

box1(xx(1)-.3e-3,-.5*pos2(1),0,2.3*xx(nop),1.5*pos2(1),tg,'b')   % pcb gnd
box1(xx(1)-.3e-3,-.5*pos2(1),tg,2.3*xx(nop),1.5*pos2(1),tg+hp,'g')   % pcb
dielectric
box1(xx(nop)-wc,-.5*pos2(1),tg+hp,2.3*xx(nop),1.5*pos2(1),tg+hp+hc,'c')
% chip dielectric
box1(xx(1)-wp/2,pos1(1)-wp/2,tg+hp,xx(1)+wp/2,pos1(1)+wp/2,tg+hp+tp,'r')
% pcb bondpad no. 1
box1(xx(1)-.3e-3,pos1(1)-wp/2,tg+hp,xx(1)-wp/2,pos1(1)+wp/2,tg+hp+tp,'m')
% wire to pcb bondpad no. 1

box1(xx(1)-wp/2,pos2(1)-wp/2,tg+hp,xx(1)+wp/2,pos2(1)+wp/2,tg+hp+tp,'r')
% pcb bondpad no. 2
box1(xx(1)-.3e-3,pos2(1)-wp/2,tg+hp,xx(1)-wp/2,pos2(1)+wp/2,tg+hp+tp,'m')
% wire to pcb bondpad no. 2

box1(xx(nop)-wc/2,pos1(nop)-wc/2,tg+hp+hc,xx(nop)+wc/2,pos1(nop)+wc/2,
tg+hp+hc+tc,'r')   % chip bondpad no. 1
box1(xx(nop)+wc/2,pos1(nop)-wc/2,tg+hp+hc,xx(nop)+.2e-3,pos1(nop)+wc/2,
tg+hp+hc+tc,'m')   % wire from chip bondpad no. 1

box1(xx(nop)-wc/2,pos2(nop)-wc/2,tg+hp+hc,xx(nop)+wc/2,pos2(nop)+wc/2,
tg+hp+hc+tc,'r')   % chip bondpad no. 2
box1(xx(nop)+wc/2,pos2(nop)-wc/2,tg+hp+hc,xx(nop)+.2e-3,pos2(nop)+wc/2,
tg+hp+hc+tc,'m')   % wire from chip bondpad no. 2


grid on

for i=1:nop-1
    [xs,ys,zs]=cylinder(rad);
    h1(i)=surf(zs*len+xx(i),xs+pos1(i),ys+d(i));

    hold on

    theta1=180/pi*atan((pos1(i+1)-pos1(i))/(xx(i+1)-xx(i)));
    rotate(h1(i),[0 0 1],theta1/50)

    axis equal
end

hold on

for i=1:nop-1
    [xs,ys,zs]=cylinder(rad);
    h2(i)=surf(zs*len+xx(i),xs+pos2(i),ys+d(i));

    hold on

    theta2=180/pi*atan((pos2(i+1)-pos2(i))/(xx(i+1)-xx(i)));
    rotate(h2(i),[0 0 1],theta2/50)

    axis equal
end plot3(xx,pos1,d,'b-',xx,pos2,d,'g-') axis equal

% Draw layers
save gen.mat disp(['whole interconnect'])
```

C.2 box1.m

```
    % Copyright © 2001
% Nader Badr
% All Rights Reserved


function box1(x0,y0,z0,x1,y1,z1,C)

fill3([x0 x1 x1 x0]',[y0 y0 y0 y0]', [z0 z0 z1 z1]',C) hold on
fill3([x0 x1 x1 x0]',[y1 y1 y1 y1]', [z0 z0 z1 z1]',C) hold on

fill3([x0 x0 x0 x0]',[y0 y1 y1 y0]', [z0 z0 z1 z1]',C) hold on
fill3([x1 x1 x1 x1]',[y0 y1 y1 y0]', [z0 z0 z1 z1]',C) hold on

fill3([x0 x1 x1 x0]',[y0 y0 y1 y1]', [z0 z0 z0 z0]',C) hold on
fill3([x0 x1 x1 x0]',[y0 y0 y1 y1]', [z1 z1 z1 z1]',C) hold on


grid on
```

C.3 msl_o_pcb.m

```
    % Copyright © 2001
% Nader Badr
% All Rights Reserved


function
msl_o_pcb(nd,condc,condbw,condp,d,erc,erp,hc,hp,len,ltc,ltp,pc,pp,rad,
ps1,ps2,tc,tg,tp,wc,wp)
% nd    Segment and node index
% len   Length of segment of line
% d         Height of bondwire from gnd

% Bond wire description file.


% This script generates input file for HSPICE. The model of bondwire is described here.
% First     W model files are generated for every small distance
% Second    HSPICE is run for each element to produce rlgc matrices


%fid=fopen(['bw_seg' num2str(nd) '.sp'],'w');
fid=fopen('bw_seg.sp','w');


fprintf(fid,'* Bond wire input file to HSPICE\n');
fprintf(fid,'* Generated on %s\n',datestr(now,-1));
fprintf(fid,'* by Nader Badr  \n\n\n\n');

fprintf(fid,'* nd=%i \t\t\t\tSegment and node index \n\n',nd);
fprintf(fid,'* condbw=%4.2e \t\tConductivity of bondwire\n',condbw);
fprintf(fid,'* condc=%4.2e \t\tConductivity of chip metal\n',condc);
fprintf(fid,'* condp=%4.2e \t\tConductivity of pcb metal\n',condp);
fprintf(fid,'* d=%4.2e m \t\t\tHeight of bondwire from gnd\n',d);
fprintf(fid,'* erc=%4.2e m \t\tDielectric constant of material \n',erc);
fprintf(fid,'* erp=%4.2e m \t\tDielectric constant of material of pcb\n',erp);
fprintf(fid,'* hc=%4.2e m \t\tThickness of dielectric layer of chip \n',hc);
```

```
fprintf(fid,'* hp=%4.2e m \t\tThickness of dielectric layer of pcb \n',hp);
fprintf(fid,'* len=%4.2e m \t\tLength of segment of line \n',len);
fprintf(fid,'* ltc=%4.2e \t\t\tLoss tangent \n',ltc);
fprintf(fid,'* ltp=%4.2e \t\t\tLoss tangent \n',ltp);
fprintf(fid,'* pc=%4.2e m \t\tExtension of chip bondpad under bondwire \n',pc);
fprintf(fid,'* pp=%4.2e m \t\tExtension of pcb bondpad under bondwire \n',pp);
fprintf(fid,'* rad=%4.2e m \t\tRadius of bondwire \n',rad);
fprintf(fid,'* ps1=%4.2e m \t\tPosition of  bw1_center starting at
pcb pad side\n\n',ps1);
fprintf(fid,'* ps2=%4.2e m \t\tPosition of  bw2_center starting at
pcb pad side\n\n',ps2);
fprintf(fid,'* tc=%4.2e m \t\tThickness of bondpad of chip \n',tc);
fprintf(fid,'* tg=%4.2e m \t\tThickness of gnd plane of pcb \n',tg);
fprintf(fid,'* tp=%4.2e m \t\tThickness of bondpad of pcb \n',tp);
fprintf(fid,'* wc=%4.2e m \t\tWidth of bondpad of chip \n',wc);
fprintf(fid,'* wp=%4.2e m \t\tWidth of bondpad of pcb \n',wp);

% bw_o_pcbpad  for bondwire over pcb bond pad


% options

fprintf(fid,'.OPTION PROBE POST\n'); fprintf(fid,'
+DELMAX=35p\n'); fprintf(fid,' +TLINLIMIT=1\n\n');


fprintf(fid,'VIMPULSE na%i gnd PULSE 1.8v 0v 5n 70p 70p 180p\n\n\n',nd);

% W element
fprintf(fid,'W%i na%i nb%i gnd na%i nb%i gnd FSmodel=segmodel_%i N=2
l=%4.2e\n\n\n',nd,nd,nd,nd+1,nd+1,nd,len);

% Materials
fprintf(fid,'.MATERIAL diel_1 DIELECTRIC ER=%4.2f  LOSSTANGENT=%4.2e\n',erp, ltp);
fprintf(fid,'.MATERIAL copperp METAL CONDUCTIVITY=%4.2e  \n',condp);
%fprintf(fid,'.MATERIAL copperbw METAL CONDUCTIVITY=%4.2e  \n\n\n',condbw);

% Shapes
%fprintf(fid,'.SHAPE  circle_1 CIRCLE RADIUS=%4.2e\n', rad);
fprintf(fid,'.SHAPE  rect_1 RECTANGLE WIDTH=%4.2e\n', wp);
fprintf(fid,' +HEIGHT=%4.2e\n\n\n',tp);

% Defines a layerstack
fprintf(fid,'.LAYERSTACK stack_1 \n');
fprintf(fid,' +LAYER=(PEC,%4.2e),\n',tg);
fprintf(fid,' +LAYER=(diel_1,%4.2e)\n\n\n',hp);

% Option Settings
fprintf(fid,'.FSOPTIONS opt1 \n');
fprintf(fid,' +ACCURACY=HIGH
\n');
fprintf(fid,' +GRIDFACTOR=4 \n');
fprintf(fid,'
+PRINTDATA=YES \n');
fprintf(fid,' +COMPUTEGO=YES \n');
fprintf(fid,' +COMPUTEGD=YES \n');
fprintf(fid,' +COMPUTERO=YES
\n');
fprintf(fid,' +COMPUTERS=YES \n\n\n');


% Model Definition
fprintf(fid,'.MODEL segmodel_%i W MODELTYPE=FieldSolver \n',nd);
fprintf(fid,' +LAYERSTACK=stack_1 FSOPTIONS=opt1,
RLGCFILE=msl.rlgc\n');
%fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e)\n',ps1,d);
```

```
%fprintf(fid,' +MATERIAL=copperbw),\n\n');
%fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e)\n',ps2,d);
%fprintf(fid,' +MATERIAL=copperbw),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(%4.2e,%4.2e)\n',ps1,hp+tg);
fprintf(fid,' +MATERIAL=copperp),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(%4.2e,%4.2e)\n',ps2,hp+tg);
fprintf(fid,' +MATERIAL=copperp),\n\n\n');


fprintf(fid,'.TRAN 70p  2n\n');
fprintf(fid,'.PROBE v(na%i)\n',nd+1);
fprintf(fid,'.END\n');

fclose(fid);
```

C.4 bw_o_pcb.m

```
    % Copyright © 2001
% Nader Badr
% All Rights Reserved


function
bw_o_pcbpad(nd,condc,condbw,condp,d,erc,erp,hc,hp,len,ltc,ltp,pc,pp,
rad,ps1,ps2,tc,tg,tp,wc,wp)
% nd    Segment and node index
% len   Length of segment of line
% d         Height of bondwire from gnd

% Bond wire description file.


% This script generates input file for HSPICE. The model of bondwire is described here.
% First     W model files are generated for every small distance
% Second    HSPICE is run for each element to produce rlgc matrices


%fid=fopen(['bw_seg' num2str(nd) '.sp'],'w');
fid=fopen('bw_seg.sp','w');


fprintf(fid,'* Bond wire input file to HSPICE\n');
fprintf(fid,'* Generated on %s\n',datestr(now,-1));
fprintf(fid,'* by Nader Badr  \n\n\n\n');

fprintf(fid,'* nd=%i \t\t\t\tSegment and node index \n\n',nd);
fprintf(fid,'* condbw=%4.2e \t\tConductivity of bondwire\n',condbw);
fprintf(fid,'* condc=%4.2e \t\tConductivity of chip metal\n',condc);
fprintf(fid,'* condp=%4.2e \t\tConductivity of pcb metal\n',condp);
fprintf(fid,'* d=%4.2e m \t\t\tHeight of bondwire from gnd\n',d);
fprintf(fid,'* erc=%4.2e m \t\tDielectric constant of material \n',erc);
fprintf(fid,'* erp=%4.2e m \t\tDielectric constant of material of pcb\n',erp);
fprintf(fid,'* hc=%4.2e m \t\tThickness of dielectric layer of chip \n',hc);
fprintf(fid,'* hp=%4.2e m \t\tThickness of dielectric layer of pcb \n',hp);
fprintf(fid,'* len=%4.2e m \t\tLength of segment of line \n',len);
fprintf(fid,'* ltc=%4.2e \t\t\tLoss tangent \n',ltc);
fprintf(fid,'* ltp=%4.2e \t\t\tLoss tangent \n',ltp);
fprintf(fid,'* pc=%4.2e m \t\tExtension of chip bondpad under bondwire \n',pc);
fprintf(fid,'* pp=%4.2e m \t\tExtension of pcb bondpad under bondwire \n',pp);
```

```
fprintf(fid,'* rad=%4.2e m \t\tRadius of bondwire \n',rad);
fprintf(fid,'* ps1=%4.2e m \t\tPosition of  bw1_center starting at pcb
pad side\n\n',ps1);
fprintf(fid,'* ps2=%4.2e m \t\tPosition of  bw2_center starting at pcb
pad side\n\n',ps2);
fprintf(fid,'* tc=%4.2e m \t\tThickness of bondpad of chip \n',tc);
fprintf(fid,'* tg=%4.2e m \t\tThickness of gnd plane of pcb \n',tg);
fprintf(fid,'* tp=%4.2e m \t\tThickness of bondpad of pcb \n',tp);
fprintf(fid,'* wc=%4.2e m \t\tWidth of bondpad of chip \n',wc);
fprintf(fid,'* wp=%4.2e m \t\tWidth of bondpad of pcb \n',wp);

% bw_o_pcbpad  for bondwire over pcb bond pad


% options

fprintf(fid,'.OPTION PROBE POST\n'); fprintf(fid,'
+DELMAX=35p\n'); fprintf(fid,' +TLINLIMIT=1\n\n');


fprintf(fid,'VIMPULSE na%i gnd PULSE 1.8v 0v 5n 70p 70p 180p\n\n\n',nd);

% W element
fprintf(fid,'W%i na%i nb%i nc%i nd%i gnd na%i nb%i nc%i nd%i gnd FSmodel=segmodel_%i N=4
l=%4.2e\n\n\n',nd,nd,nd,nd,nd,nd,nd+1,nd+1,nd+1,nd+1,nd,len);

% Materials
fprintf(fid,'.MATERIAL diel_1 DIELECTRIC ER=%4.2f  LOSSTANGENT=%4.2e\n',erp, ltp);
fprintf(fid,'.MATERIAL copperp METAL CONDUCTIVITY=%4.2e  \n',condp);
fprintf(fid,'.MATERIAL copperbw METAL CONDUCTIVITY=%4.2e  \n\n\n',condbw);

% Shapes
fprintf(fid,'.SHAPE  circle_1 CIRCLE RADIUS=%4.2e\n', rad);
fprintf(fid,'.SHAPE  rect_1 RECTANGLE WIDTH=%4.2e\n', wp);
fprintf(fid,' +HEIGHT=%4.2e\n\n\n',tp);

% Defines a layerstack
fprintf(fid,'.LAYERSTACK stack_1 \n');
fprintf(fid,' +LAYER=(PEC,%4.2e),\n',tg);
fprintf(fid,' +LAYER=(diel_1,%4.2e)\n\n\n',hp);

% Option Settings
fprintf(fid,'.FSOPTIONS opt1 \n');
fprintf(fid,'
+ACCURACY=HIGH\n');
fprintf(fid,' +GRIDFACTOR=4 \n');
fprintf(fid,' +PRINTDATA=YES \n');
fprintf(fid,' +COMPUTEGO=YES
\n'); fprintf(fid,' +COMPUTEGD=YES \n');
fprintf(fid,'+COMPUTERO=YES \n');
fprintf(fid,' +COMPUTERS=YES
\n\n\n');


% Model Definition
fprintf(fid,'.MODEL segmodel_%i W MODELTYPE=FieldSolver \n',nd);
fprintf(fid,' +LAYERSTACK=stack_1 FSOPTIONS=opt1,
RLGCFILE=seg.rlgc\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e)\n',ps1,d);
fprintf(fid,' +MATERIAL=copperbw),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e)\n',ps2,d);
fprintf(fid,' +MATERIAL=copperbw),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(%4.2e,%4.2e)\n',ps1,hp+tg);
fprintf(fid,' +MATERIAL=copperp),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(%4.2e,%4.2e)\n',ps2,hp+tg);
fprintf(fid,' +MATERIAL=copperp),\n\n\n');
```

```
fprintf(fid,'.TRAN 70p  2n\n');
fprintf(fid,'.PROBE v(na%i)\n',nd+1);
fprintf(fid,'.END\n');

fclose(fid);
```

C.5 bw_o_diel.m

```
    % Copyright © 2001
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function
bw_o_diel(nd,condc,condbw,condp,d,erc,erp,hc,hp,len,ltc,ltp,pc,pp,rad,
ps1,ps2,tc,tg,tp,wc,wp)
% nd    Segment and node index
% len   Length of segment of line
% d         Height of bondwire from gnd

% Bond wire description file.


% This script generates input file for HSPICE. The model of bondwire is described here.
% First     W model files are generated for every small distance
% Second    HSPICE is run for each element to

% bw_odiel   for bondwire over chip pad


%fid=fopen(['bw_seg' num2str(nd) '.sp'],'w');
fid=fopen('bw_seg.sp','w');


fprintf(fid,'* Bond wire input file to HSPICE\n');
fprintf(fid,'* Generated on %s\n',datestr(now,-1));
fprintf(fid,'* by Nader Badr  \n\n\n\n');


fprintf(fid,'* nd=%i \t\t\t\tSegment and node index \n\n',nd);
fprintf(fid,'* condbw=%4.2e \t\tConductivity of bondwire\n',condbw);
fprintf(fid,'* condc=%4.2e \t\tConductivity of chip metal\n',condc);
fprintf(fid,'* condp=%4.2e \t\tConductivity of pcb metal\n',condp);
fprintf(fid,'* d=%4.2e m \t\t\tHeight of bondwire from gnd\n',d);
fprintf(fid,'* erc=%4.2e m \t\tDielectric constant of material \n',erc);
fprintf(fid,'* erp=%4.2e m \t\tDielectric constant of material of pcb\n',erp);
fprintf(fid,'* hc=%4.2e m \t\tThickness of dielectric layer of chip \n',hc);
fprintf(fid,'* hp=%4.2e m \t\tThickness of dielectric layer of pcb \n',hp);
fprintf(fid,'* len=%4.2e m \t\tLength of segment of line \n',len);
fprintf(fid,'* ltc=%4.2e \t\t\tLoss tangent \n',ltc);
fprintf(fid,'* ltp=%4.2e \t\t\tLoss tangent \n',ltp);
fprintf(fid,'* pc=%4.2e m \t\tExtension of chip bondpad under bondwire \n',pc);
fprintf(fid,'* pp=%4.2e m \t\tExtension of pcb bondpad under bondwire \n',pp);
fprintf(fid,'* rad=%4.2e m \t\tRadius of bondwire \n',rad);
fprintf(fid,'* ps1=%4.2e m \t\tPosition of  bw1_center starting at
pcb pad side\n\n',ps1);
fprintf(fid,'* ps2=%4.2e m \t\tPosition of  bw2_center starting at
pcb pad side\n\n',ps2);
```

```
fprintf(fid,'* tc=%4.2e m \t\tThickness of bondpad of chip \n',tc);
fprintf(fid,'* tg=%4.2e m \t\tThickness of gnd plane of pcb \n',tg);
fprintf(fid,'* tp=%4.2e m \t\tThickness of bondpad of pcb \n',tp);
fprintf(fid,'* wc=%4.2e m \t\tWidth of bondpad of chip \n',wc);
fprintf(fid,'* wp=%4.2e m \t\tWidth of bondpad of pcb \n',wp);

% options

fprintf(fid,'.OPTION PROBE POST\n'); fprintf(fid,'
+DELMAX=35p\n'); fprintf(fid,' +TLINLIMIT=1\n\n');


fprintf(fid,'VIMPULSE na%i gnd PULSE 1.8v 0v 5n 70p 70p 180p\n\n\n',nd);

% W element
fprintf(fid,'W%i na%i nb%i gnd na%i nb%i gnd FSmodel=segmodel_%i N=2 l=
%4.2e\n\n\n',nd,nd,nd,nd+1,nd+1,nd,len);

% Materials
fprintf(fid,'.MATERIAL diel_1 DIELECTRIC ER=%4.2f  LOSSTANGENT=%4.2e\n',erp, ltp);
fprintf(fid,'.MATERIAL copperbw METAL CONDUCTIVITY=%4.2e  \n\n\n',condbw);

% Shapes
fprintf(fid,'.SHAPE  circle_1 CIRCLE RADIUS=%4.2e\n', rad);
%fprintf(fid,'.SHAPE  rect_%i RECTANGLE WIDTH=%4.2e\n',nd, w2);
%fprintf(fid,' +HEIGHT=%4.2e\n\n\n',t2);

% Defines a lyerstack
fprintf(fid,'.LAYERSTACK stack_1 \n');
fprintf(fid,' +LAYER=(PEC,%4.3e)\n',tg);
fprintf(fid,' +LAYER=(diel_1,%4.2e)\n\n\n',hp);

% Option Settings
fprintf(fid,'.FSOPTIONS opt1 \n');
fprintf(fid,' +ACCURACY=HIGH
\n');
fprintf(fid,' +GRIDFACTOR=4 \n');
fprintf(fid,'
+PRINTDATA=YES \n');
fprintf(fid,' +COMPUTEGO=YES \n');
fprintf(fid,' +COMPUTEGD=YES \n');
fprintf(fid,' +COMPUTERO=YES
\n');
fprintf(fid,' +COMPUTERS=YES \n\n\n');


% Model Definition
fprintf(fid,'.MODEL segmodel_%i W MODELTYPE=FieldSolver \n',nd);
fprintf(fid,' +LAYERSTACK=stack_1 FSOPTIONS=opt1,
RLGCFILE=seg.rlgc\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e)\n',ps1,d);
fprintf(fid,' +MATERIAL=copperbw),\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e)\n',ps2,d);
fprintf(fid,' +MATERIAL=copperbw),\n');



fprintf(fid,'.TRAN 70p  2n\n');
fprintf(fid,'.PROBE v(na%i)\n',nd+1);
fprintf(fid,'.END\n');

fclose(fid);
```

C.6 bw_o_chippad.m

```
    % Copyright © 2001
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 function bw_o_chippad(nd,condc,condbw,condp,d,erc,erp,hc,hp,len,ltc,ltp,
 pc,pp,rad,ps1,ps2,tc,tg,tp,wc,wp)
% nd    Segment and node index
% len   Length of segment of line
% d         Height of bondwire from gnd

% Bond wire description file.


% This script generates input file for HSPICE. The model of bondwire
is described here.
% First     W model files are generated for every small distance
% Second    HSPICE is run for each element to produce rlgc matrices


%fid=fopen(['bw_seg' num2str(nd) '.sp'],'w');
fid=fopen('bw_seg.sp','w');


fprintf(fid,'* Bond wire input file to HSPICE\n');
fprintf(fid,'* Generated on %s\n',datestr(now,-1));
fprintf(fid,'* by Nader Badr  \n\n\n\n');

fprintf(fid,'* nd=%i \t\t\t\tSegment and node index \n\n',nd);
fprintf(fid,'* condbw=%4.2e \t\tConductivity of bondwire\n',condbw);
fprintf(fid,'* condc=%4.2e \t\tConductivity of chip metal\n',condc);
fprintf(fid,'* condp=%4.2e \t\tConductivity of pcb metal\n',condp);
fprintf(fid,'* d=%4.2e m \t\t\tHeight of bondwire from gnd\n',d);
fprintf(fid,'* erc=%4.2e m \t\tDielectric constant of material \n',erc);
fprintf(fid,'* erp=%4.2e m \t\tDielectric constant of material of pcb\n',erp);
fprintf(fid,'* hc=%4.2e m \t\tThickness of dielectric layer of chip \n',hc);
fprintf(fid,'* hp=%4.2e m \t\tThickness of dielectric layer of pcb \n',hp);
fprintf(fid,'* len=%4.2e m \t\tLength of segment of line \n',len);
fprintf(fid,'* ltc=%4.2e \t\t\tLoss tangent \n',ltc);
fprintf(fid,'* ltp=%4.2e \t\t\tLoss tangent \n',ltp);
fprintf(fid,'* pc=%4.2e m \t\tExtension of chip bondpad under bondwire \n',pc);
fprintf(fid,'* pp=%4.2e m \t\tExtension of pcb bondpad under bondwire \n',pp);
fprintf(fid,'* rad=%4.2e m \t\tRadius of bondwire \n',rad);
fprintf(fid,'* ps1=%4.2e m \t\tPosition of  bw1_center starting at pcb
pad side\n\n',ps1);
fprintf(fid,'* ps2=%4.2e m \t\tPosition of  bw2_center starting at pcb
pad side\n\n',ps2);
fprintf(fid,'* tc=%4.2e m \t\tThickness of bondpad of chip \n',tc);
fprintf(fid,'* tg=%4.2e m \t\tThickness of gnd plane of pcb \n',tg);
fprintf(fid,'* tp=%4.2e m \t\tThickness of bondpad of pcb \n',tp);
fprintf(fid,'* wc=%4.2e m \t\tWidth of bondpad of chip \n',wc);
fprintf(fid,'* wp=%4.2e m \t\tWidth of bondpad of pcb \n',wp);


% bw_o_chippad  for bondwire over chip bond pad


% options

fprintf(fid,'.OPTION PROBE POST   \n'); fprintf(fid,'
+DELMAX=35p\n'); fprintf(fid,' +TLINLIMIT=1\n\n');


fprintf(fid,'VIMPULSE na%i gnd PULSE 1.8v 0v 5n 70p 70p 180p\n\n\n',nd);
```

```
% W element
fprintf(fid,'W%i na%i nb%i nc%i nd%i gnd na%i nb%i nc%i nd%i gnd FSmodel=segmodel_%i
N=4 l=%4.2e\n\n\n',nd,nd,nd,nd,nd,nd+1,nd+1,nd+1,nd+1,nd,len);

% Materials
fprintf(fid,'.MATERIAL diel_1 DIELECTRIC ER=%4.2f  LOSSTANGENT=%4.2e\n',erp, ltp);
fprintf(fid,'.MATERIAL diel_2 DIELECTRIC ER=%4.2f  LOSSTANGENT=%4.2e\n',erc, ltc);
fprintf(fid,'.MATERIAL copperc METAL CONDUCTIVITY=%4.2e  \n',condc);
fprintf(fid,'.MATERIAL copperbw METAL CONDUCTIVITY=%4.2e  \n\n\n',condbw);

% Shapes
fprintf(fid,'.SHAPE  circle_1 CIRCLE RADIUS=%4.2e\n', rad);
fprintf(fid,'.SHAPE  rect_1 RECTANGLE WIDTH=%4.2e,\n', wc);
fprintf(fid,' +HEIGHT=%4.2e\n\n\n',tc);

% Defines a layerstack
fprintf(fid,'.LAYERSTACK stack_1 \n');
fprintf(fid,' +LAYER=(PEC,%4.2e),\n',tg);
fprintf(fid,' +LAYER=(diel_1,%4.2e)\n',hp);
fprintf(fid,' +LAYER=(diel_2,%4.2e)\n\n\n',hc);

% Option Settings
fprintf(fid,'.FSOPTIONS opt1 \n'); fprintf(fid,' +ACCURACY=HIGH
\n'); fprintf(fid,' +GRIDFACTOR=4 \n'); fprintf(fid,'
+PRINTDATA=YES \n'); fprintf(fid,' +COMPUTEGO=YES \n');
fprintf(fid,' +COMPUTEGD=YES \n'); fprintf(fid,' +COMPUTERO=YES
\n'); fprintf(fid,' +COMPUTERS=YES \n\n\n');


% Model Definition
fprintf(fid,'.MODEL segmodel_%i W MODELTYPE=FieldSolver \n',nd);
fprintf(fid,' +LAYERSTACK=stack_1 FSOPTIONS=opt1,
RLGCFILE=seg.rlgc\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e),\n',ps1,d);
fprintf(fid,' +MATERIAL=copperbw),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(%4.2e,%4.2e),\n',ps2,d);
fprintf(fid,' +MATERIAL=copperbw),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(%4.2e,%4.2e)\n',ps1,hc+tg);
fprintf(fid,' +MATERIAL=copperc),\n\n');
fprintf(fid,' +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(%4.2e,%4.2e)\n',ps2,hc+tg);
fprintf(fid,' +MATERIAL=copperc),\n\n\n');




fprintf(fid,'.TRAN 70p  2n\n');
fprintf(fid,'.PROBE v(na%i)\n',nd+1);
fprintf(fid,'.END\n');

fclose(fid);
```

C.7 bw_o_pcbpad.sp


```
* Bond wire input file to HSPICE
* Generated on 27-Jan-2003 09:06:35
```

```
* by Nader Badr


* nd=          Segment and node index

* condbw=      Conductivity of bondwire
* condc=       Conductivity of chip metal
* condp=       Conductivity of pcb metal
* d=           Height of bondwire from gnd
* erc=         Dielectric constant of material
* erp=         Dielectric constant of material of pcb
* hc=          Thickness of dielectric layer of chip
* hp=          Thickness of dielectric layer of pcb
* len=         Length of segment of line
* ltc=         Loss tangent
* ltp=         Loss tangent
* pc=          Extension of chip bondpad under bondwire
* pp=          Extension of pcb bondpad under bondwire
* rad=         Radius of bondwire
* ps1=         Position of  bw1_center starting at pcb pad side

* ps2=        Position of  bw2_center starting at pcb pad side

* tc=          Thickness of bondpad of chip
* tg=          Thickness of gnd plane of pcb
* tp=          Thickness of bondpad of pcb
* wc=          Width of bondpad of chip
* wp=          Width of bondpad of pcb
.OPTION PROBE POST
 +DELMAX=35p
 +TLINLIMIT=1

VIMPULSE na23 gnd PULSE 1.8v 0v 5n 70p 70p 180p


W23 na23 nb23 nc23 nd23 gnd na24 nb24 nc24 nd24 gnd
FSmodel=segmodel_23 N=4 l=4.50e-06


.MATERIAL diel_1 DIELECTRIC ER=3.05  LOSSTANGENT=2.70e-03
.MATERIAL copperp METAL CONDUCTIVITY=5.72e+07 .MATERIAL copperbw
METAL CONDUCTIVITY=5.72e+07


.SHAPE  circle_1 CIRCLE RADIUS=1.00e-05 .SHAPE  rect_1 RECTANGLE
WIDTH=2.00e-04
 +HEIGHT=3.50e-05


.LAYERSTACK stack_1
 +LAYER=(PEC,3.50e-05),
 +LAYER=(diel_1,7.32e-04)


.FSOPTIONS opt1
 +ACCURACY=HIGH
 +GRIDFACTOR=4
 +PRINTDATA=YES
 +COMPUTEGO=YES
 +COMPUTEGD=YES
 +COMPUTERO=YES
 +COMPUTERS=YES


.MODEL segmodel_23 W MODELTYPE=FieldSolver
```

```
+LAYERSTACK=stack_1 FSOPTIONS=opt1, RLGCFILE=seg.rlgc
+CONDUCTOR=(SHAPE=circle_1,ORIGIN=(1.31e-04,9.24e-04)
+MATERIAL=copperbw),

+CONDUCTOR=(SHAPE=circle_1,ORIGIN=(4.69e-04,9.24e-04)
+MATERIAL=copperbw),

+CONDUCTOR=(SHAPE=rect_1,ORIGIN=(1.31e-04,7.67e-04)
+MATERIAL=copperp),

+CONDUCTOR=(SHAPE=rect_1,ORIGIN=(4.69e-04,7.67e-04)
+MATERIAL=copperp),


.TRAN 70p  2n .PROBE v(na24) .END
```

C.8 bw_o_diel.sp

```
    % Copyright © 2001
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* Bond wire input file to HSPICE
* Generated on 27-Jan-2003 09:06:57
* by Nader Badr


* nd=          Segment and node index

* condbw=      Conductivity of bondwire
* condc=       Conductivity of chip metal
* condp=       Conductivity of pcb metal
* d=           Height of bondwire from gnd
* erc=         Dielectric constant of material
* erp=         Dielectric constant of material of pcb
* hc=          Thickness of dielectric layer of chip
* hp=          Thickness of dielectric layer of pcb
* len=         Length of segment of line
* ltc=         Loss tangent
* ltp=         Loss tangent
* pc=          Extension of chip bondpad under bondwire
* pp=          Extension of pcb bondpad under bondwire
* rad=         Radius of bondwire
* ps1=         Position of  bw1_center starting at pcb pad side

* ps2=        Position of  bw2_center starting at pcb pad side

* tc=          Thickness of bondpad of chip
* tg=          Thickness of gnd plane of pcb
* tp=          Thickness of bondpad of pcb
* wc=          Width of bondpad of chip
* wp=          Width of bondpad of pcb
.OPTION PROBE POST
 +DELMAX=35p
 +TLINLIMIT=1

VIMPULSE na90 gnd PULSE 1.8v 0v 5n 70p 70p 180p
```

```
W90 na90 nb90 gnd na91 nb91 gnd FSmodel=segmodel_90 N=2 l=4.50e-06


.MATERIAL diel_1 DIELECTRIC ER=3.05  LOSSTANGENT=2.70e-03
.MATERIAL copperbw METAL CONDUCTIVITY=5.72e+07


.SHAPE  circle_1 CIRCLE RADIUS=1.00e-05 .LAYERSTACK stack_1
 +LAYER=(PEC,3.500e-05)
 +LAYER=(diel_1,7.32e-04)


.FSOPTIONS opt1
 +ACCURACY=HIGH
 +GRIDFACTOR=4
 +PRINTDATA=YES
 +COMPUTEGO=YES
 +COMPUTEGD=YES
 +COMPUTERO=YES
 +COMPUTERS=YES


.MODEL segmodel_90 W MODELTYPE=FieldSolver
 +LAYERSTACK=stack_1 FSOPTIONS=opt1, RLGCFILE=seg.rlgc
 +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(2.24e-04,8.38e-04)
 +MATERIAL=copperbw),
 +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(3.76e-04,8.38e-04)
 +MATERIAL=copperbw),
.TRAN 70p  2n .PROBE v(na91) .END
```

C.9 bw_o_chippad.sp

```
    % Copyright © 2001
% Nader Badr
% All Rights Reserved


* Bond wire input file to HSPICE
* Generated on 27-Jan-2003 09:07:01
* by Nader Badr


* nd=          Segment and node index

* condbw=      Conductivity of bondwire
* condc=       Conductivity of chip metal
* condp=       Conductivity of pcb metal
* d=           Height of bondwire from gnd
* erc=         Dielectric constant of material
* erp=         Dielectric constant of material of pcb
* hc=          Thickness of dielectric layer of chip
* hp=          Thickness of dielectric layer of pcb
* len=         Length of segment of line
* ltc=         Loss tangent
* ltp=         Loss tangent
* pc=          Extension of chip bondpad under bondwire
* pp=          Extension of pcb bondpad under bondwire
* rad=         Radius of bondwire
* ps1=         Position of  bw1_center starting at pcb pad side
```

```
* ps2=        Position of  bw2_center starting at pcb pad side

* tc=         Thickness of bondpad of chip
* tg=         Thickness of gnd plane of pcb
* tp=         Thickness of bondpad of pcb
* wc=         Width of bondpad of chip
* wp=         Width of bondpad of pcb
.OPTION PROBE POST
 +DELMAX=35p
 +TLINLIMIT=1

VIMPULSE na100 gnd PULSE 1.8v 0v 5n 70p 70p 180p


W100 na100 nb100 nc100 nd100 gnd na101 nb101 nc101 nd101 gnd
FSmodel=segmodel_100 N=4 l=4.50e-06


.MATERIAL diel_1 DIELECTRIC ER=3.05  LOSSTANGENT=2.70e-03
.MATERIAL diel_2 DIELECTRIC ER=4.10  LOSSTANGENT=2.70e-03
.MATERIAL copperc METAL CONDUCTIVITY=5.72e+07 .MATERIAL copperbw
METAL CONDUCTIVITY=5.72e+07


.SHAPE  circle_1 CIRCLE RADIUS=1.00e-05 .SHAPE  rect_1 RECTANGLE
WIDTH=7.50e-05,
 +HEIGHT=9.90e-08


.LAYERSTACK stack_1
 +LAYER=(PEC,3.50e-05),
 +LAYER=(diel_1,7.32e-04)
 +LAYER=(diel_2,4.00e-04)


.FSOPTIONS opt1
 +ACCURACY=HIGH
 +GRIDFACTOR=4
 +PRINTDATA=YES
 +COMPUTEGO=YES
 +COMPUTEGD=YES
 +COMPUTERO=YES
 +COMPUTERS=YES


.MODEL segmodel_100 W MODELTYPE=FieldSolver
 +LAYERSTACK=stack_1 FSOPTIONS=opt1, RLGCFILE=seg.rlgc
 +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(2.38e-04,8.22e-04),
 +MATERIAL=copperbw),

 +CONDUCTOR=(SHAPE=circle_1,ORIGIN=(3.63e-04,8.22e-04),
 +MATERIAL=copperbw),

 +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(2.38e-04,4.35e-04)
 +MATERIAL=copperc),

 +CONDUCTOR=(SHAPE=rect_1,ORIGIN=(3.63e-04,4.35e-04)
 +MATERIAL=copperc),


.TRAN 70p  2n .PROBE v(na101) .END
```

C.10 msl.rlgc

```
    % Copyright © 2001
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*SYSTEM_NAME : segmodel_0 *
*       Half Space, air
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_0 W MODELTYPE=RLGC, N=2 + Lo =  6.17224e-07 +
2.79076e-07  6.17224e-07 + Co =  4.49870e-11 +      -1.72676e-11
4.49870e-11 + Ro =  2.49748e+00 +       0.00000e+00  2.49748e+00 +
Go =  0.00000e+00 +      -0.00000e+00  0.00000e+00 + Rs =
7.54565e-04 +      -3.66360e-05  7.54565e-04 + Gd =  3.81593e-13 +
-1.46469e-13  3.81593e-13
```

C.11 seg.rlgc

```
    % Copyright © 2001
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*SYSTEM_NAME : segmodel_1
*
*       Half Space, air
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_1 W MODELTYPE=RLGC, N=4
+ Lo =  8.23556e-07
+       2.86665e-07  8.20179e-07
+       5.58297e-07  2.99289e-07  6.13894e-07
+       2.67712e-07  5.56693e-07  2.79552e-07  6.13991e-07
+ Co =  3.58533e-11
+      -2.59307e-13  3.61139e-11
+      -3.17548e-11 -3.10353e-12  7.36426e-11
+      -6.81435e-13 -3.09675e-11 -1.39719e-11  7.17802e-11
+ Ro =  5.13143e+01
+       0.00000e+00  5.13143e+01
+       0.00000e+00  0.00000e+00  2.49747e+00
+       0.00000e+00  0.00000e+00  0.00000e+00  2.49747e+00
+ Go =  0.00000e+00
```

```
+      -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00 -0.00000e+00  0.00000e+00
+ Rs =  5.52622e-03
+       6.54639e-05  5.48518e-03
+      -2.06209e-04  3.25467e-04  9.96774e-04
+      -2.82383e-04 -2.27713e-04 -5.88470e-05  9.92858e-04
+ Gd =  3.04118e-13
+      -2.19952e-15  3.06329e-13
+      -2.69354e-13 -2.63251e-14  6.24658e-13
+      -5.78013e-15 -2.62676e-13 -1.18514e-13  6.08861e-13

*SYSTEM_NAME : segmodel_2
*
*       Half Space, air
*  ---------------------------------- Z = 0.000767
*       diel_1   H = 0.000732
*  ---------------------------------- Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ---------------------------------- Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_2 W MODELTYPE=RLGC, N=4
+ Lo =  9.13723e-07
+       3.06609e-07  9.07344e-07
+       5.19761e-07  3.27893e-07  6.13504e-07
+       2.74919e-07  5.16697e-07  2.95569e-07  6.13585e-07
+ Co =  2.41058e-11
+      -4.49933e-13  2.44774e-11
+      -1.93912e-11 -3.64679e-12  6.27135e-11
+      -8.09211e-13 -1.84365e-11 -1.55111e-11  6.03940e-11
+ Ro =  5.13143e+01
+       0.00000e+00  5.13143e+01
+       0.00000e+00  0.00000e+00  2.49747e+00
+       0.00000e+00  0.00000e+00  0.00000e+00  2.49747e+00
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00 -0.00000e+00  0.00000e+00
+ Rs =  4.02138e-03
+       2.62283e-05  4.02332e-03
+       5.19958e-05  1.83622e-04  9.38636e-04
+      -1.91272e-04  5.11856e-05 -5.60484e-05  9.35904e-04
+ Gd =  2.04472e-13
+      -3.81646e-15  2.07624e-13
+      -1.64482e-13 -3.09331e-14  5.31954e-13
+      -6.86397e-15 -1.56384e-13 -1.31570e-13  5.12280e-13

*SYSTEM_NAME : segmodel_3
*
*       Half Space, air
*  ---------------------------------- Z = 0.000767
*       diel_1   H = 0.000732
*  ---------------------------------- Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ---------------------------------- Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_3 W MODELTYPE=RLGC, N=4
+ Lo =  1.00565e-06
+       3.34261e-07  9.99365e-07
+       4.32532e-07  3.48852e-07  6.11739e-07
+       2.75813e-07  4.29454e-07  3.14855e-07  6.11838e-07
+ Co =  1.65785e-11
```

```
+      -1.32014e-12  1.70352e-11
+      -1.00191e-11 -3.87957e-12  5.56402e-11
+      -1.09545e-12 -9.14958e-12 -1.83589e-11  5.34003e-11
+ Ro =  5.13143e+01
+       0.00000e+00  5.13143e+01
+       0.00000e+00  0.00000e+00  2.49747e+00
+       0.00000e+00  0.00000e+00  0.00000e+00  2.49747e+00
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00 -0.00000e+00  0.00000e+00
+ Rs =  3.24386e-03
+       6.26517e-05  3.28184e-03
+       1.31005e-04  7.57801e-05  9.16040e-04
+      -9.38620e-05  1.40944e-04 -5.97752e-05  9.12373e-04
+ Gd =  1.40623e-13
+      -1.11978e-14  1.44498e-13
+      -8.49847e-14 -3.29077e-14  4.71957e-13
+      -9.29189e-15 -7.76095e-14 -1.55726e-13  4.52957e-13

*SYSTEM_NAME : segmodel_4
*
*       Half Space, air
*  ---------------------------------- Z = 0.000767
*       diel_1   H = 0.000732
*  ---------------------------------- Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ---------------------------------- Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_4 W MODELTYPE=RLGC, N=2
+ Lo =  1.05503e-06
+       3.73034e-07  1.05503e-06
+ Co =  1.32639e-11
+      -3.39532e-12  1.32639e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+ Rs =  2.94210e-03
+       4.39651e-07  2.94210e-03
+ Gd =  1.12509e-13
+      -2.88002e-14  1.12509e-13

*SYSTEM_NAME : segmodel_5
*
*       Half Space, air
*  ---------------------------------- Z = 0.000767
*       diel_1   H = 0.000732
*  ---------------------------------- Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ---------------------------------- Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_5 W MODELTYPE=RLGC, N=2
+ Lo =  1.06870e-06
+       4.06523e-07  1.06870e-06
+ Co =  1.31065e-11
+      -3.87696e-12  1.31065e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+ Rs =  2.94402e-03
```

```
+       3.76804e-07  2.94402e-03
+ Gd =  1.11173e-13
+      -3.28855e-14  1.11173e-13

*SYSTEM_NAME : segmodel_6
*
*       Half Space, air
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_6 W MODELTYPE=RLGC, N=2
+ Lo =  1.06863e-06
+       4.28982e-07  1.06863e-06
+ Co =  1.33096e-11
+      -4.23739e-12  1.33096e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+ Rs =  2.94668e-03
+       3.65364e-07  2.94668e-03
+ Gd =  1.12896e-13
+      -3.59428e-14  1.12896e-13

*SYSTEM_NAME : segmodel_7
*
*       Half Space, air
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_7 W MODELTYPE=RLGC, N=2
+ Lo =  1.05482e-06
+       4.42684e-07  1.05482e-06
+ Co =  1.38710e-11
+      -4.52054e-12  1.38710e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+ Rs =  2.95085e-03
+       3.98482e-07  2.95084e-03
+ Gd =  1.17658e-13
+      -3.83446e-14  1.17658e-13

*SYSTEM_NAME : segmodel_8
*
*       Half Space, air
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_8 W MODELTYPE=RLGC, N=2
```

```
+ Lo =  1.03419e-06
+       4.51961e-07  1.03419e-06
+ Co =  1.48206e-11
+      -4.75766e-12  1.48206e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+ Rs =  2.95686e-03
+       4.53096e-07  2.95685e-03
+ Gd =  1.25713e-13
+      -4.03559e-14  1.25713e-13

*SYSTEM_NAME : segmodel_9
*
*       Half Space, air
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_9 W MODELTYPE=RLGC, N=2
+ Lo =  1.01486e-06
+       4.67848e-07  1.01486e-06
+ Co =  1.64746e-11
+      -5.25837e-12  1.64746e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
+ Rs =  2.96668e-03
+       4.58444e-07  2.96668e-03
+ Gd =  1.39742e-13
+      -4.46031e-14  1.39742e-13

*SYSTEM_NAME : segmodel_10
*
*       Half Space, air
*  ------------------------------------ Z = 0.001167
*       diel_2   H = 0.0004
*  ------------------------------------ Z = 0.000767
*       diel_1   H = 0.000732
*  ------------------------------------ Z = 3.5e-05
*  //// Bottom Ground Plane ///////////
*  ------------------------------------ Z = 0

* L(H/m), C(F/m), Ro(Ohm/m), Go(S/m), Rs(Ohm/(m*sqrt(Hz)), Gd(S/(m*Hz))

.MODEL segmodel_10 W MODELTYPE=RLGC, N=4
+ Lo =  1.00904e-06
+       5.06528e-07  1.00910e-06
+       2.21635e-07  2.18870e-07  7.38779e-07
+       2.09677e-07  2.21991e-07  3.83993e-07  7.38785e-07
+ Co =  5.77353e-11
+      -3.03920e-11  5.79739e-11
+      -6.39302e-12 -5.07314e-12  6.51298e-11
+      -4.37475e-12 -6.47059e-12 -3.05837e-11  6.48906e-11
+ Ro =  5.13144e+01
+       0.00000e+00  5.13144e+01
+       0.00000e+00  0.00000e+00  2.35455e+03
+       0.00000e+00  0.00000e+00  0.00000e+00  2.35455e+03
+ Go =  0.00000e+00
+      -0.00000e+00  0.00000e+00
```

```
+      -0.00000e+00 -0.00000e+00  0.00000e+00
+      -0.00000e+00 -0.00000e+00 -0.00000e+00  0.00000e+00
+ Rs =  1.48708e-04
+       8.66604e-07  1.47992e-04
+       1.67387e-05  5.97593e-06  1.21887e-03
+      -2.57939e-06  1.11513e-05 -1.27744e-04  1.21887e-03
+ Gd =  6.52971e-13
+      -3.43726e-13  6.55669e-13
+      -7.23034e-14 -5.73759e-14  7.36601e-13
+      -4.94772e-14 -7.31806e-14 -3.45894e-13  7.33895e-13
```

C.12 bw_sub.lib

```
    % Copyright © 2001
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* Complete Bond wire model input file to HSPICE
* Generated on 27-Jan-2003 13:06:44
* by Nader Badr


* nd=          Segment and node index

* condbw=      Conductivity of bondwire
* condc=       Conductivity of chip metal
* condp=       Conductivity of pcb metal
* d=           Height of bondwire from gnd
* erc=         Dielectric constant of material
* erp=         Dielectric constant of material of pcb
* hc=          Thickness of dielectric layer of chip
* hp=          Thickness of dielectric layer of pcb
* len=         Length of segment of line
* ltc=         Loss tangent
* ltp=         Loss tangent
* pc=          Extension of chip bondpad under bondwire
* pp=          Extension of pcb bondpad under bondwire
* rad=         Radius of bondwire
* ps1=         Position of  bw1_center starting at pcb pad side

* ps2=        Position of  bw2_center starting at pcb pad side

* tc=          Thickness of bondpad of chip
* tg=          Thickness of gnd plane of pcb
* tp=          Thickness of bondpad of pcb
* wc=          Width of bondpad of chip
* wp=          Width of bondpad of pcb

.LIB bw1

.SUBCKT bw1 na1 nb1 na11 nb11


.inc '/home/nbadr/RESEARCH/channel1/gml_bondwire/seg.rlgc' Ra1 na1
nc1 1e-5 Rb1 nb1 nd1 1e-5

* pos1=1.00e-04                Position of  bw1_center from pcb pad side
* pos2=5.00e-04                Position of  bw2_center from pcb pad side
W1 na1 nb1 nc1 nd1 gnd na2 nb2 nc2 nd2 gnd +RLGCmodel=segmodel_1
```

```
N=4 l=4.50e-05

* pos1=1.15e-04                Position of  bw1_center from pcb pad side
* pos2=4.85e-04                Position of  bw2_center from pcb pad side
W2 na2 nb2 nc2 nd2 gnd na3 nb3 nc3 nd3 gnd +RLGCmodel=segmodel_2
N=4 l=4.50e-05

* pos1=1.31e-04                Position of  bw1_center from pcb pad side
* pos2=4.69e-04                Position of  bw2_center from pcb pad side
W3 na3 nb3 nc3 nd3 gnd na4 nb4 nc4 nd4 gnd +RLGCmodel=segmodel_3
N=4 l=4.50e-05

Ra4 nc4 gnd 100G Rb4 nd4 gnd 100G

* pos1=1.46e-04                Position of  bw1_center from pcb pad side
* pos2=4.54e-04                Position of  bw2_center from pcb pad side
W4 na4 nb4 gnd na5 nb5 gnd +RLGCmodel=segmodel_4 N=2 l=4.50e-05

* pos1=1.61e-04                Position of  bw1_center from pcb pad side
* pos2=4.39e-04                Position of  bw2_center from pcb pad side
W5 na5 nb5 gnd na6 nb6 gnd +RLGCmodel=segmodel_5 N=2 l=4.50e-05

* pos1=1.76e-04                Position of  bw1_center from pcb pad side
* pos2=4.24e-04                Position of  bw2_center from pcb pad side
W6 na6 nb6 gnd na7 nb7 gnd +RLGCmodel=segmodel_6 N=2 l=4.50e-05

* pos1=1.92e-04                Position of  bw1_center from pcb pad side
* pos2=4.08e-04                Position of  bw2_center from pcb pad side
W7 na7 nb7 gnd na8 nb8 gnd +RLGCmodel=segmodel_7 N=2 l=4.50e-05

* pos1=2.07e-04                Position of  bw1_center from pcb pad side
* pos2=3.93e-04                Position of  bw2_center from pcb pad side
W8 na8 nb8 gnd na9 nb9 gnd +RLGCmodel=segmodel_8 N=2 l=4.50e-05

* pos1=2.22e-04                Position of  bw1_center from pcb pad side
* pos2=3.78e-04                Position of  bw2_center from pcb pad side
W9 na9 nb9 gnd na10 nb10 gnd +RLGCmodel=segmodel_9 N=2 l=4.50e-05

Ra10 nc10 gnd 100G Rb10 nd10 gnd 100G

* pos1=2.38e-04                Position of  bw1_center from pcb pad side
* pos2=3.63e-04                Position of  bw2_center from pcb pad side
W10 na10 nb10 nc10 nd10 gnd na11 nb11 nc11 nd11 gnd
+RLGCmodel=segmodel_10 N=4 l=4.50e-05

Ra11 na11 nc11 1e-5 Rb11 nb11 nd11 1e-5

.ENDS bw1

.ENDL bw1
```

C.13 converts.m

```
function converts(filename1,filename2,nelem) Lo=zeros(4,4,nelem);
Co=zeros(4,4,nelem); Ro=zeros(4,4,nelem); Go=zeros(4,4,nelem);
Rs=zeros(4,4,nelem); Gd=zeros(4,4,nelem);

seg=1; for cc=1:1, fid = fopen(filename1, 'r');

% Read one line at a time
while feof(fid)==0
    line = fgetl(fid);
    len_line=length(line);
   line=[line blanks(15)];
   len_line=length(line);
    ind= findstr(line,'.MODEL');

    if(isempty(ind)==0 & ind ~=0),
      indn= findstr(line,'N=');
        element_str=line(indn+2:indn+4);
        el_no=str2num(element_str);

        for a=1:el_no
        line = fgetl(fid);
        Lo(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Co(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Ro(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Go(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Rs(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Gd(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        seg=seg+1;

    end
end

% Upper and lower matrices made symmetric
fclose(fid); end

for c=1:seg-1
   for b=1:el_no
      for a=1:el_no
         if(a>b)
                Lo(b,a,c)=Lo(a,b,c);
                Co(b,a,c)=Co(a,b,c);
                Gd(b,a,c)=Gd(a,b,c);
         end
      end
   end
 end


fid = fopen(filename2, 'r');
```

```
% Read one line at a time
while feof(fid)==0
    line = fgetl(fid);
    len_line=length(line);
   line=[line blanks(15)];
   len_line=length(line);
    ind= findstr(line,'.MODEL');

    if(isempty(ind)==0 & ind ~=0),
      indn= findstr(line,'N=');
        element_str=line(indn+2:indn+4);
        el_no=str2num(element_str);

        for a=1:el_no
        line = fgetl(fid);
        Lo(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Co(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Ro(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Go(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Rs(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        for a=1:el_no
        line = fgetl(fid);
        Gd(a,1:a,seg)=str2num(line(8:max(size(line))));
        end
        seg=seg+1;

    end
end

% Upper and lower matrices made symmetric

for c=1:seg-1
   for b=1:el_no
      for a=1:el_no
         if(a>b)
                Lo(b,a,c)=Lo(a,b,c);
                Co(b,a,c)=Co(a,b,c);
                Gd(b,a,c)=Gd(a,b,c);
         end
      end
   end
 end



fseek(fid,0,-1); f=5e9

R=Ro+sqrt(f)*Rs; G=Go+f*Gd;
Zo=sqrt((R+i*2*pi*f*Lo)./(G+i*2*pi*f*Co));
Zop1_bw1(1:nelem,1)=Zo(1,1,1:nelem);
Zop2_bw1(1:nelem,1)=Zo(2,2,1:nelem);

% Odd mode characteristic impedance
```

```
for c=1:seg-1
   for b=1:el_no
      Ld(b,b,c)=Lo(b,b,c);
      for a=1:el_no
            if(b~=a)
                Ld(b,b,c)=Ld(b,b,c)-abs(Lo(a,b,c));
           end
      end
   end
end


for c=1:seg-1
   for b=1:el_no
        Cd(b,b,c)=0;
        Cd(b,b,c)=sum(abs(Co(:,b,c)));
   end
end

for c=1:seg-1
   for b=1:el_no
        Gdd(b,b,c)=0;
        Gdd(b,b,c)=sum(abs(Gd(:,b,c)));
   end
end

Rodd=Ro+sqrt(f)*Rs;

%save test1.mat
Gddf=Go+f*Gdd;

Zod=sqrt((Rodd+i*2*pi*f*Ld)./(Gddf+i*2*pi*f*Cd));
Zodp1_bw1(1:nelem,1)=Zod(1,1,1:nelem);
Zodp2_bw1(1:nelem,1)=Zod(2,2,1:nelem);


% Even mode characteristic impedance


for c=1:seg-1
   for b=1:el_no
      Le(b,b,c)=0;
      Le(b,b,c)=sum(abs(Lo(:,b,c)));
   end
end


for c=1:seg-1
   for b=1:el_no
      for a=1:el_no
        Ce(b,b,c)=Co(b,b,c);
            if(b~=a)
                Ce(b,b,c)=Ce(b,b,c)-abs(Co(a,b,c));
          end
        end
   end
end

for c=1:seg-1
   for b=1:el_no
        Gde(b,b,c)=0;
        Gde(b,b,c)=sum(abs(Gd(:,b,c)));
   end
end
```

```
Re=Ro+sqrt(f)*Rs; Gdef=Go+f*Gde;

Ze=sqrt((Re+i*2*pi*f*Le)./(Gdef+i*2*pi*f*Ce));
Zep1_bw1(1:nelem,1)=Ze(1,1,1:nelem);
Zep2_bw1(1:nelem,1)=Ze(2,2,1:nelem);



save seg1.mat

figure(2),plot(abs(Zop1_bw1),'ro-') hold on
figure(2),plot(abs(Zodp1_bw1),'kd-') hold on
figure(2),plot(abs(Zep1_bw1),'g^-') hold on figure(2),legend('Zo1
o-','Zodd1 d-','Ze ^-',0)

%plot(R,y,'o')
fclose(fid);
```

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